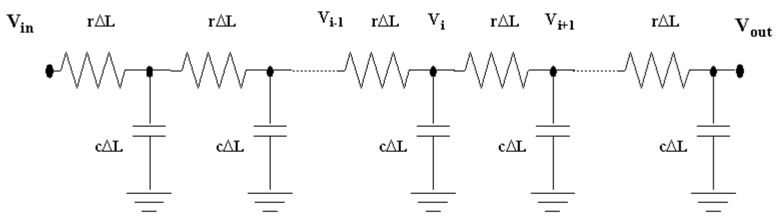
EECS 427
Lecture 19: Interconnects
Readings: 9.2-9.4

Reminders

- One more deadline
  - Finish your project by Dec. 14
  - Schematic, layout, simulations, and final assembly (CAD9)
  - Final report and project presentation (HW5)
- Quiz 2 during the lecture period on Wednesday
  - Extended office hours this week
    - Monday 3–3:30 pm and after 5:30 pm
    - Tuesday 3–4 pm and after 5 pm
  - Bring one-page cheat sheet and calculator

The Elmore Delay RC Chain



$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Wire Model

Assume: Wire modeled by N equal-length segments

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

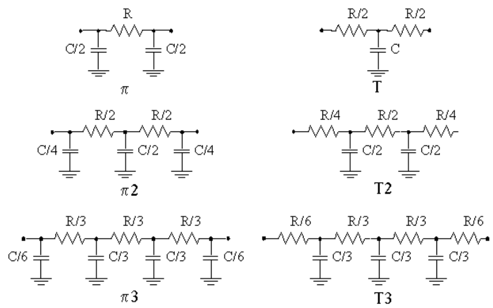
For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

RC-Model

Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks: Points of Interest.



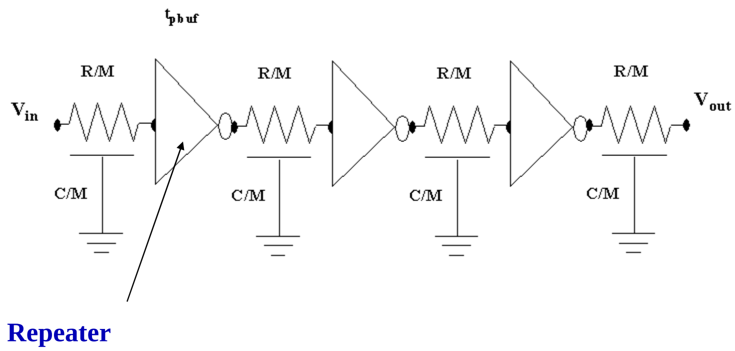
The Global Wire Problem

$$T_d = 0.377 R_w C_w + 0.693 \left(R_d C_{out} + R_d C_w + R_w C_{out} \right)$$

Challenges

- No further improvements to be expected after the introduction of Copper (superconducting, optical?)
- Design solutions
  - Use of fat wires
  - Insert repeaters — but might become prohibitive (power, area)
  - Efficient chip floorplanning
- Towards "communication-based" design
  - How to deal with latency?
  - Is synchronicity an absolute necessity?

Reducing RC-delay



$$M = L\sqrt{\frac{0.38rc}{t_{pbuf}}}$$ (chapter 5)

Repeater Insertion (Revisited)

Taking the repeater loading into account

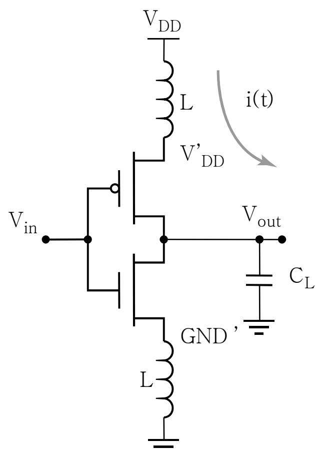
$$m_{opt} = L\sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma+1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

$$s_{opt} = \sqrt{\frac{R_dc}{rC_d}}$$

For a given technology and a given interconnect layer, there exists an optimal length of the wire segments between repeaters. The delay of these wire segments is independent of the routing layer!

$$L_{crit} = \frac{L}{m_{opt}} = \sqrt{\frac{t_{p1}}{0.38rc}} \qquad t_{p,crit} = \frac{t_{p,min}}{m_{opt}} = 2\left(1+\sqrt{\frac{0.69}{0.38(1+\gamma)}}\right)t_{p1}$$

L di/dt

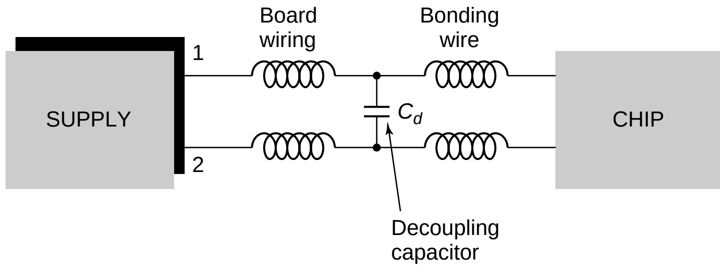


Impact of inductance on supply voltages:
• Change in current induces a change in voltage
• Longer supply lines have larger L

Dealing with Ldi/dt

- **Separate power pins for I/O pads and chip core.**
- **Multiple power and ground pin**s.
- **Careful selection of the positions of the power and ground pins on the packag**e.
- **Increase the rise and fall times** of the off-chip signals to the maximum extent allowable.
- **Schedule current-consuming transitions.**
- **Use advanced packaging technologies.**
- **Add decoupling capacitances on the board.**
- **Add decoupling capacitances on the chip.**

Decoupling Capacitors



Decoupling capacitors are added:
- on the board (right under the supply pins)
- on the chip (under the supply straps, near large buffers)

Quiz 2 Review

- ----- Power and Energy -----
- Lecture 11: sources of power and energy dissipation -- dynamic, leakage, and short-circuit
- Lecture 12: dynamic power reduction – logic design, lower VDD + (sizing, lower Vt), multi-VDD, frequency scaling, frequency + voltage scaling, clock gating, architectural transformation (lower VDD + parallel, pipelining)
- Lecture 13: leakage power reduction – multi-Vt, stacking (body effect + DIBL effect), state forcing, sleep transistor (MTCMOS, boosted sleep, sizing tradeoffs), dynamic body bias (FBB active, RBB sleep)

- ----- Timing and sequential elements -----
- Lecture 14: basics – timing parameters (setup, hold, tcq, tdq), non-idealities (skew, jitter), effects on timing (setup constraint, hold constraint), latch timing (slack passing/borrowing)
- Lecture 15: registers and latches – master-slave (reduced clock loading, clock overlap), C^2MOS (overlap immune), TSPC (single phase), pulse latch (fast)

- ----- Memory -----
- Lecture 16: 6T SRAM (read and write), row decoding, column decoding, sense amp
- Lecture 17: 3T DRAM, 1T DRAM, reliability and yield, sources of power and energy dissipation

- ----- Interconnects -----
- Lecture 18 and 19: coupling, sizing drivers (for speed, or power), IR drop, interconnect delay, repeater insertion, Ldi/dt noise