EECS 427
Lecture 2: Design Rules & Layout Intro

Reading: 2.3, Insert A, Weste 1.5, 3.3 (handouts)

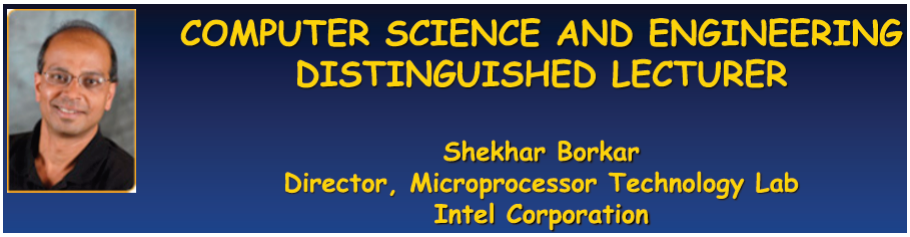
With thanks to Irwin/Narayanan

Logistics

- CAD1 due this Wednesday, Sept. 16 at 7pm
- HW1 due next Monday, Sept. 21 at the beginning of lecture
- HW1 readings: 3.5, 12.2, 5.4, 6.2.3

- Wei-Hsiang's office hours are M/Th 4-6pm and Tu 6:30-7:30pm (CAD1 Questions are encouraged!)
- Discussions start this week: Tu 5:30-6:30pm

Seminar Announcement



Tuesday 4:00-5:00 pm 1670 CSE

Last Time

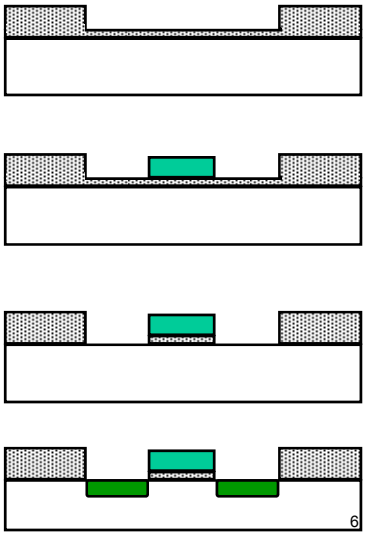
- Course intro and logistics
- Processing flow: helps you to picture how the layout relates to the physical silicon implementation

Outline

- Design rules introduction
  - What are they and why do we have them?
- You will quickly memorize our own design rules!

Self-Aligned Gates

1. Create thin oxide in the "active" regions, thick elsewhere
2. Deposit polysilicon
3. Etch thin oxide from active region (poly acts as a mask for the diffusion)
4. Implant dopant



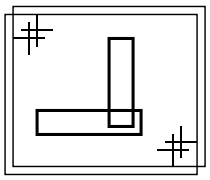
Design Rules

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum feature size (transistor gate length)
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

Why Have Design Rules?

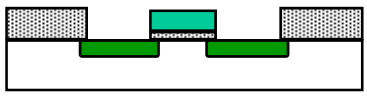
- To be able to tolerate some level of fabrication errors such as

1. Mask misalignment



2. Dust

3. Process parameters (e.g., lateral diffusion)

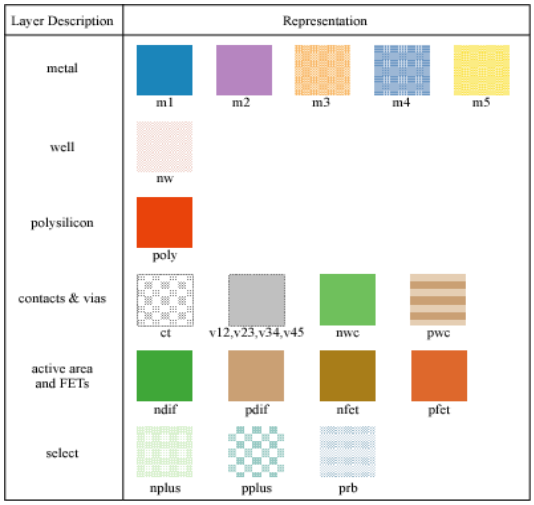


4. Rough surfaces

Typical CMOS Process Layers

Layers	Key Points	Layout
Well (n, p)	N-well process → p-type wafer (no p-well)	NW
Active Area (n+, p+) → Select (n+, p+)	Active area determines transistor location Select is where n+ and p+ ion implantation occurs; also used to create well and substrate contacts	RX BP
Polysilicon	Poly overlapping with active = transistor	PC
Metal1		M1
Metal2		M2
Contact to Active	All contacts/vias are the same size (eases processing)	CA
Contact to Poly		
Via		Vx (various colors)

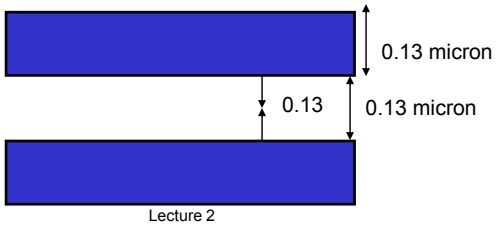
Layers in the book's 0.25 μm CMOS process



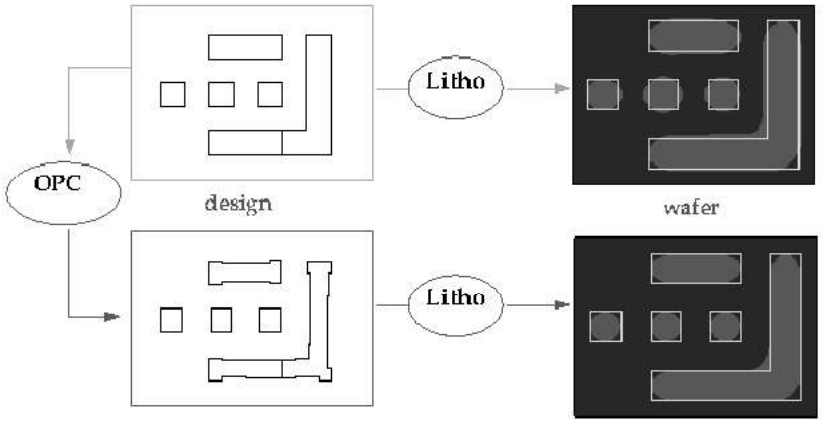
The book's process is NOT exactly the same as the one we will be using

Intra-Layer Design Rule

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



Optical Proximity Correction (OPC)



Nick Cobb, UCB

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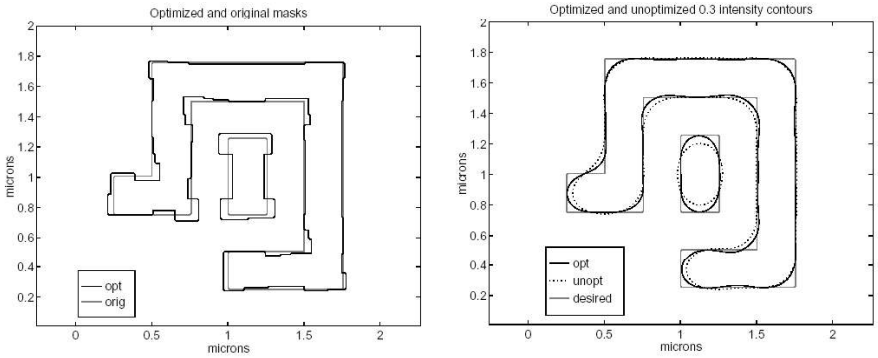
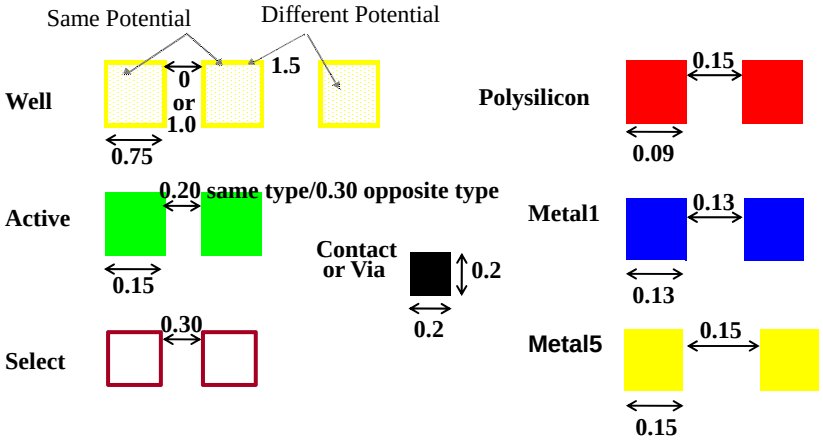


Nick Cobb, UCB

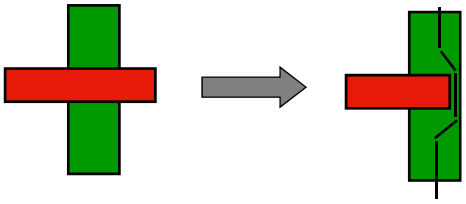
Intra-Layer Design Rules



Inter-Layer Design Rule

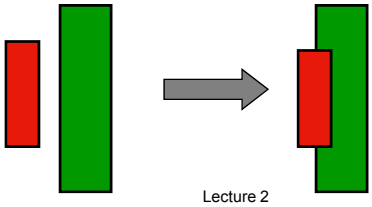
Transistor rules – transistor formed by overlap of diffusion (also called active) and poly layers

Transistors



Catastrophic error, source and drain are shorted

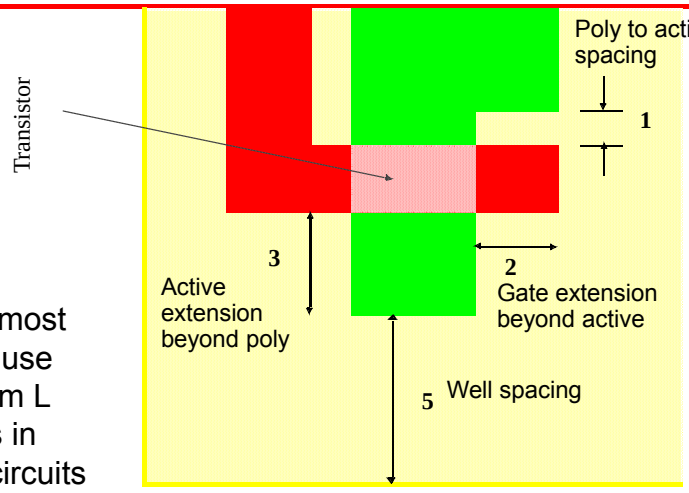
Unrelated Poly & Diffusion



Diffusion region is more resistive (narrower), but still working

But never use diffusion for routing!

Transistor Layout

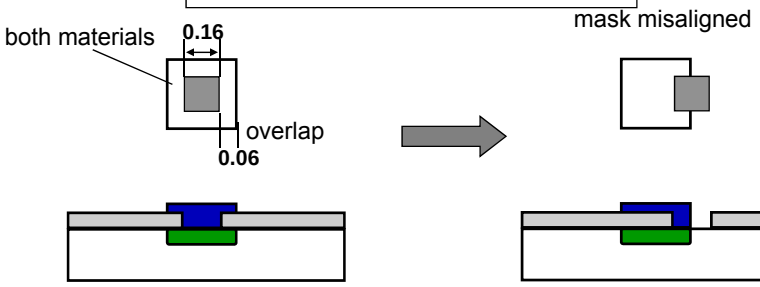


We'll almost always use minimum L devices in digital circuits

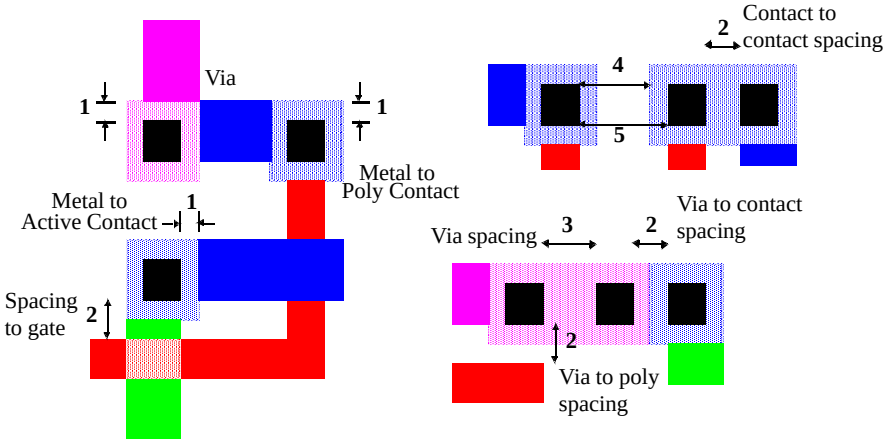
Contacts

Contact and via rules

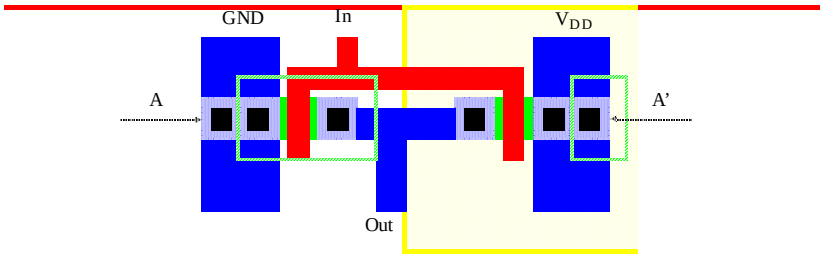
M1 contact to p-diffusion M1 contact to n-diffusion M1 contact to poly	Contact Mask
Mx contact to My	Via Masks



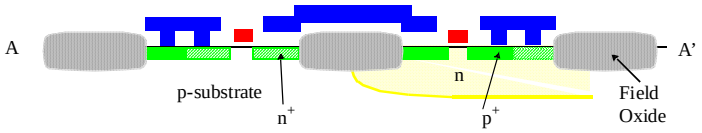
Vias and Contacts



CMOS Inverter Layout

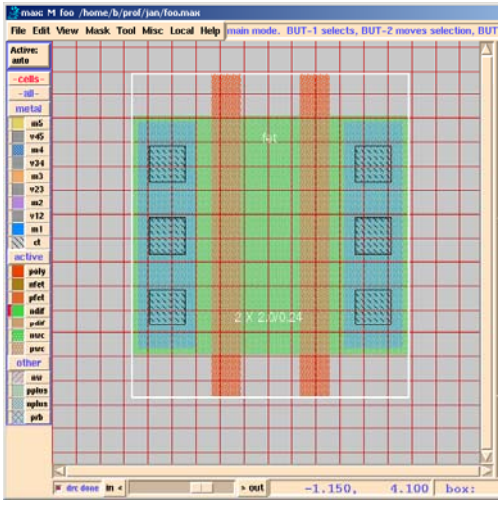


(a) Layout



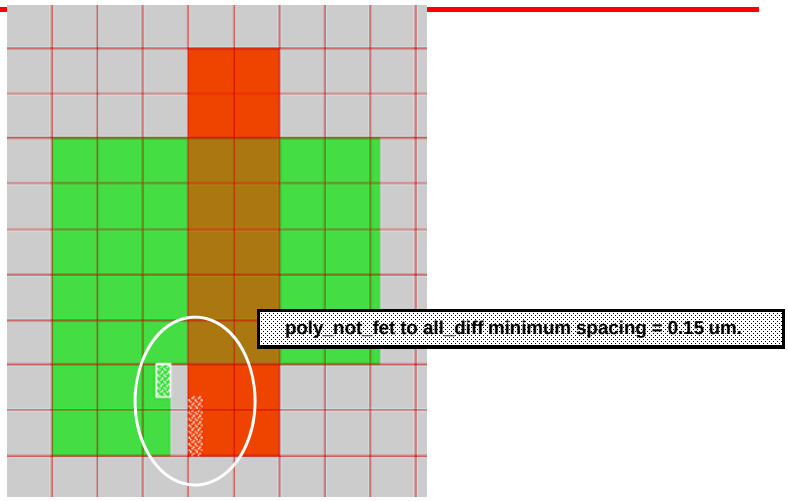
(b) Cross-Section along A-A'

Example of Layout Editor

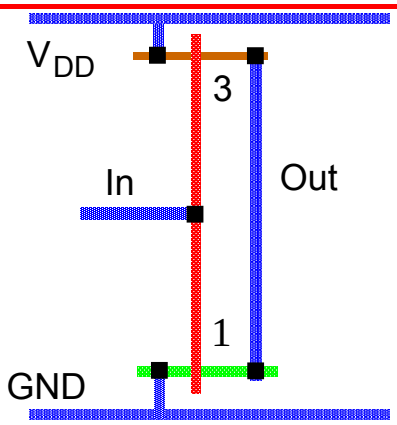


2 series connected devices

Design Rule Check (DRC)



Stick Diagram



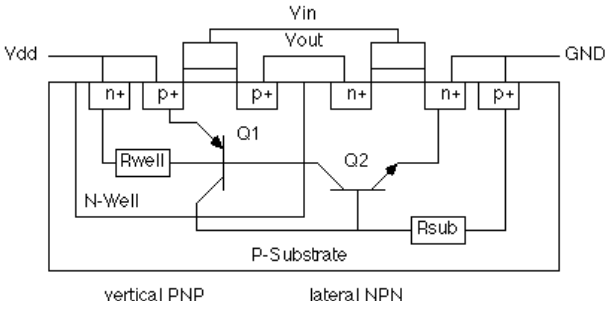
- Dimensionless layout entities
- Only topology is important

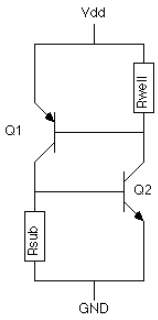
Stick diagram of inverter

Antenna rules

- Charging in semiconductor processing
  - Many process steps use plasmas, charged particles
  - Charge collects on conducting poly, metal surfaces
  - Large amounts of charge on poly can create huge E-fields across the thin gate oxide and lead to breakdown
  - Amount of charge collected is proportional to area of conductors
- Important ratio: antenna ratio defined as:
  - $(A_{poly} + A_{M1} + \ldots) / A_{gate\_ox}$
  - A_{Mx} = metal x area electrically connected to node
    - This is very conservative as higher levels of metal can alleviate the problem
  - If a diode is attached along the line, antenna rules are relaxed
    - Provides a low impedance path for large amounts of charge to be removed from the conductor

Latch-up



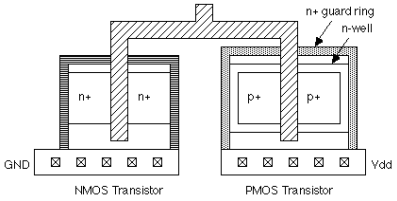


- Most commonly a problem for I/O pads with big drivers, large currents, possible voltage overshoots

How to avoid latch-up

- Reduce the gain product $\beta 1 \times \beta 2$
  - move n-well and n+ source/drain farther apart increases width of the base of Q2 and reduces gain $\beta 2$ → also reduces circuit density
  - buried n+ layer in well reduces gain of Q1
- Reduce the well and substrate resistances, producing lower voltage drops
  - higher substrate doping level reduces Rsub
  - reduce Rwell by making low resistance contact to GND
  - guard rings around p- and/or n-well, with frequent contacts to the rings, reduces the parasitic resistances

Aim for 1 well or substrate plug per gate



Summary

- Design rules = contract between process engineer and designer
  - Balance between yield and performance
- Next time: CMOS review
- Readings: 5.4, 6.2
- Tutorial 2 in discussion on Tuesday
- CAD2 will be assigned on Wednesday
- Form a group in two weeks!
- Shekhar Borkar's Seminar on Tuesday 4-5pm 1670 CSE