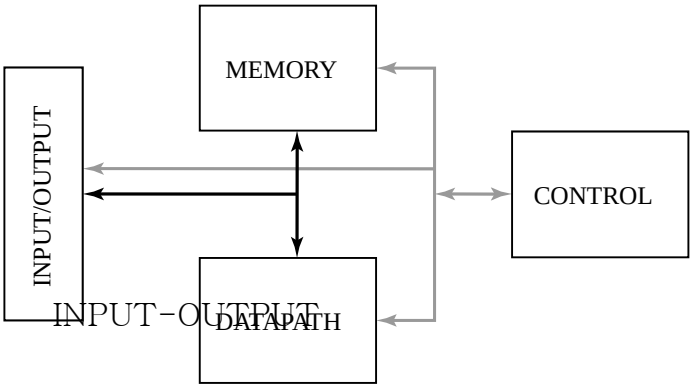
EECS 427
Lecture 20: Design and Synthesis
Readings: 8.1-8.4, Inserts E, F

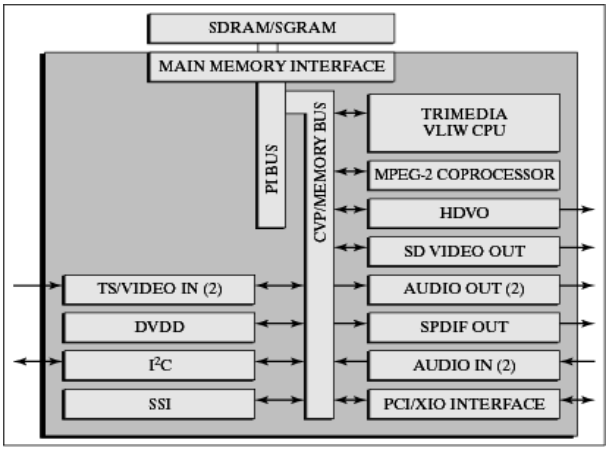
Reminders

- One more deadline
  - Finish your project by Dec. 14
  - Schematic, layout, simulations, and final assembly (CAD9)
  - Final report and project presentation (HW5)
- Office hours this week
  - Mon 3 – 4 pm
  - Tue 5 – 6 pm
  - Sun 3 – 6 pm
- Remaining lectures
  - 11/30 Monday: Design and synthesis
  - 12/2 Wednesday: Design for test
  - 12/7 Monday: Zhengya's research
  - 12/9 Wednesday: Clock and power distribution
  - 12/14 Monday: Project presentation

A Simple Processor

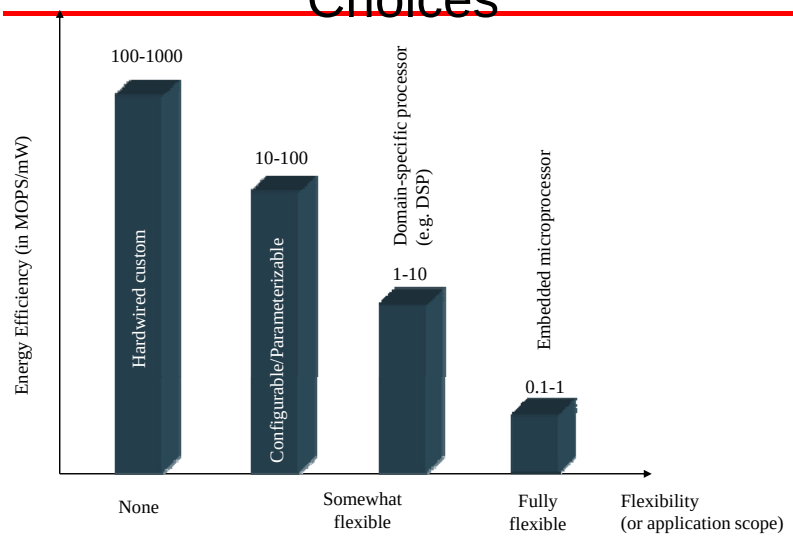


A System-on-a-Chip: Example

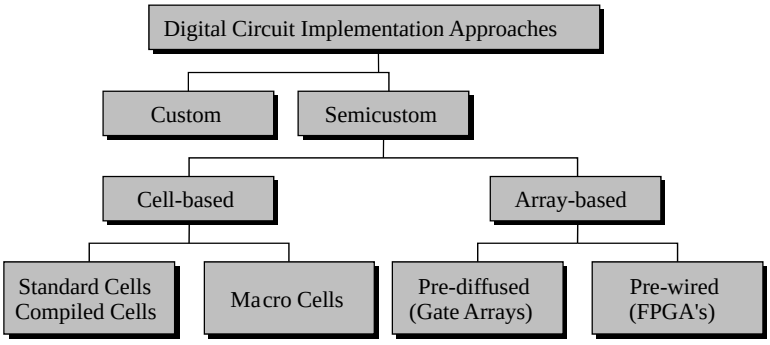


Courtesy: Philips

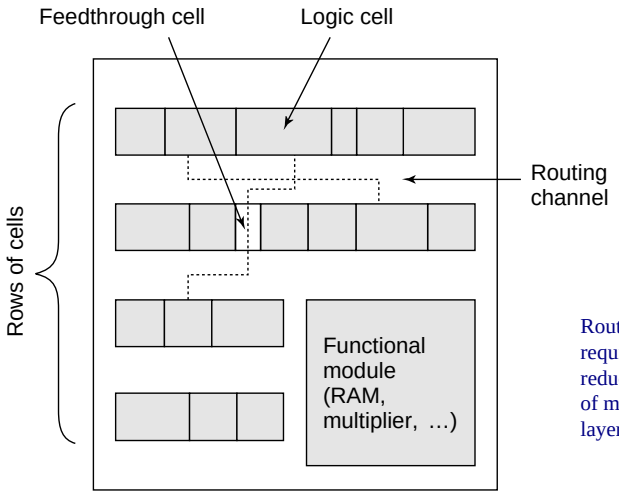
Impact of Implementation Choices



Implementation Choices

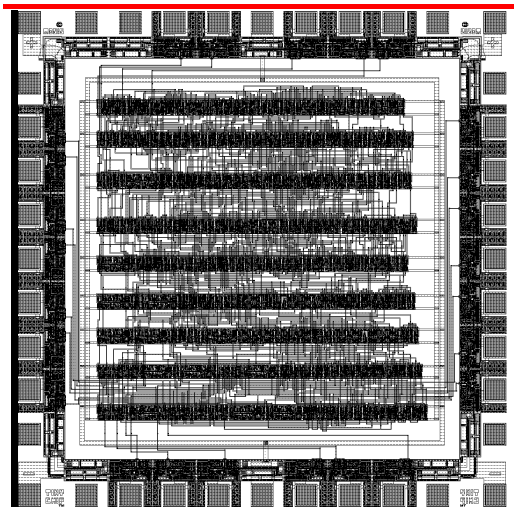


Cell-based Design



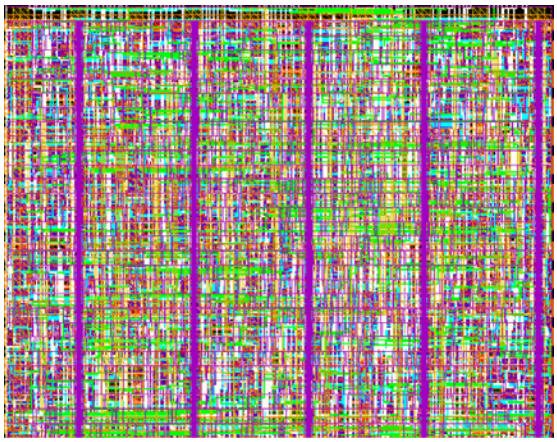
Routing channel requirements are reduced by presence of more interconnect layers

Standard Cell — Example



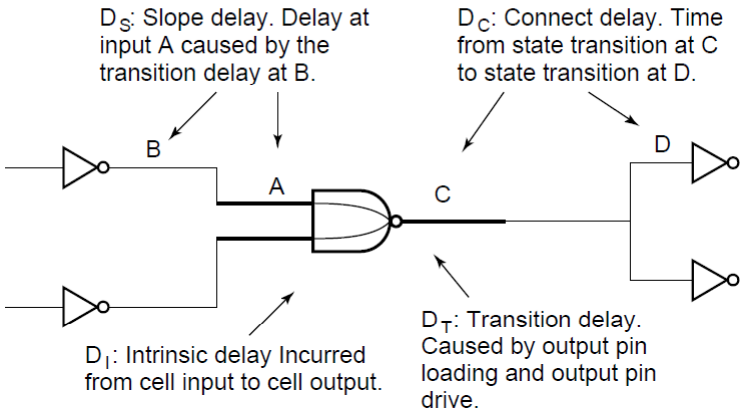
[Brodersen92]

Standard Cell

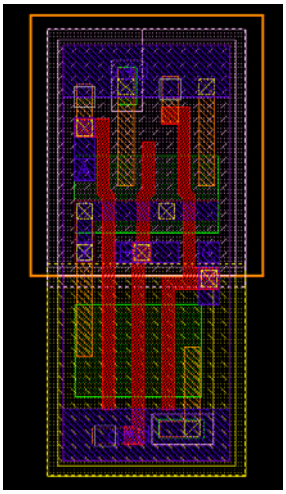


Cell-structure hidden under interconnect layers

Timing Model



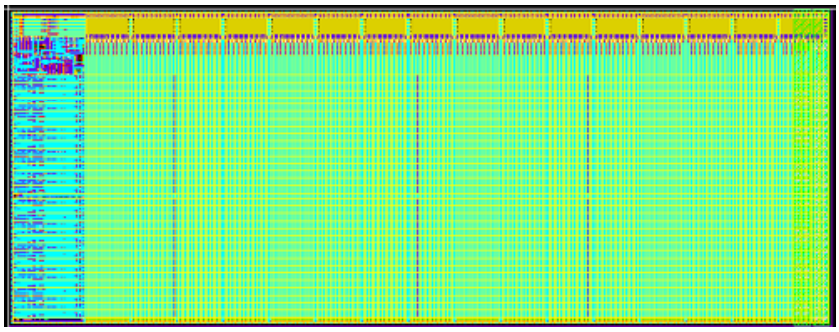
Standard Cell - Example



Path	1.2V - 125°C	1.6V - 40°C
$In1—t_{pLH}$	$0.073+7.98C+0.317T$	$0.020+2.73C+0.253T$
$In1—t_{pHL}$	$0.069+8.43C+0.364T$	$0.018+2.14C+0.292T$
$In2—t_{pLH}$	$0.101+7.97C+0.318T$	$0.026+2.38C+0.255T$
$In2—t_{pHL}$	$0.097+8.42C+0.325T$	$0.023+2.14C+0.269T$
$In3—t_{pLH}$	$0.120+8.00C+0.318T$	$0.031+2.37C+0.258T$
$In3—t_{pHL}$	$0.110+8.41C+0.280T$	$0.027+2.15C+0.223T$

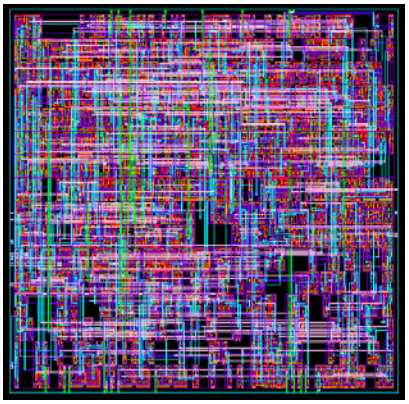
3-input NAND cell
(from ST Microelectronics):
C = Load capacitance
T = input rise/fall time

MacroModules



256×32 (or 8192 bit) SRAM
Generated by hard-macro module generator

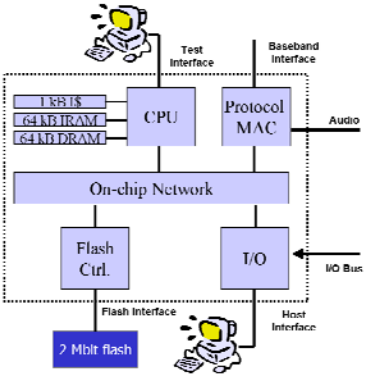
“Soft” MacroModules

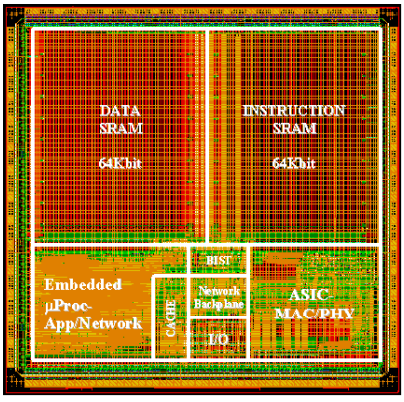


```
string mat = "booth";
directive (multtype = mat);
output signed [16] Z = A * B;
```

Synopsys DesignCompiler

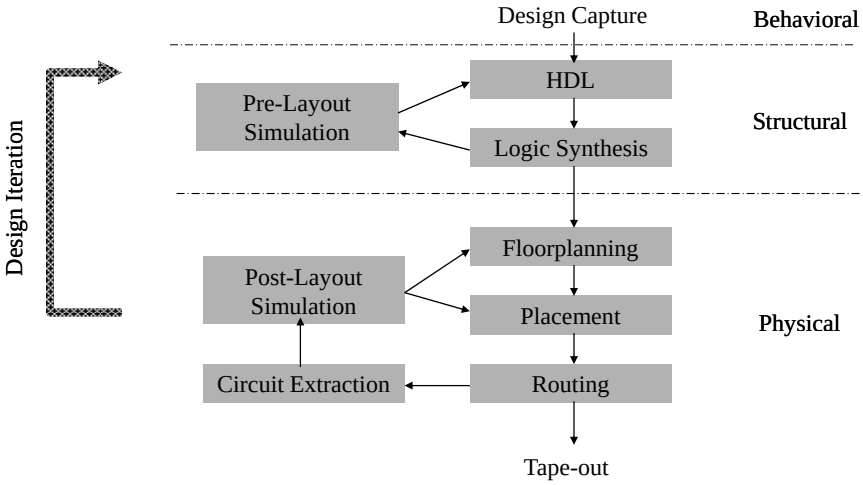
“Intellectual Property”



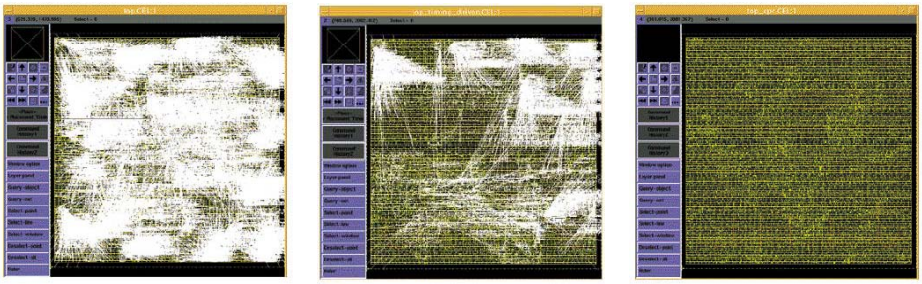


A Protocol Processor for Wireless

Semicustom Design Flow



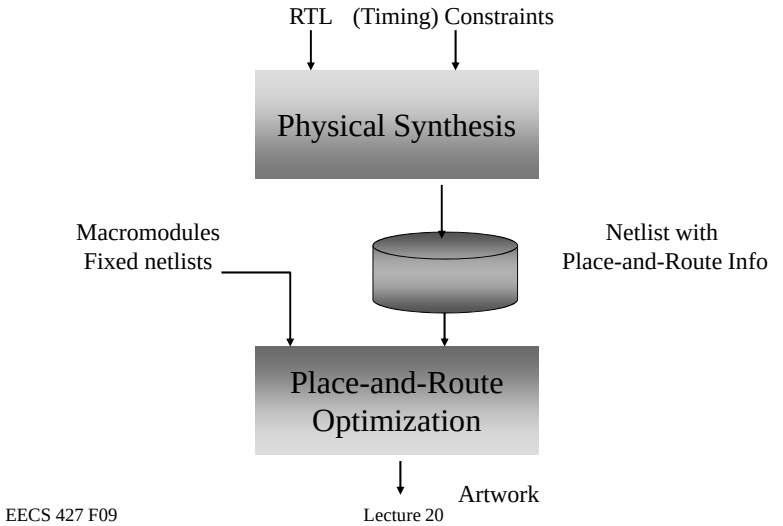
The "Design Closure" Problem



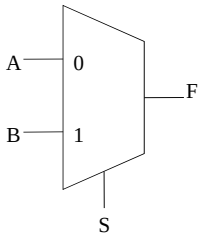
Iterative Removal of Timing Violations (white lines)

Courtesy Synopsys

Integrating Synthesis with Physical Design

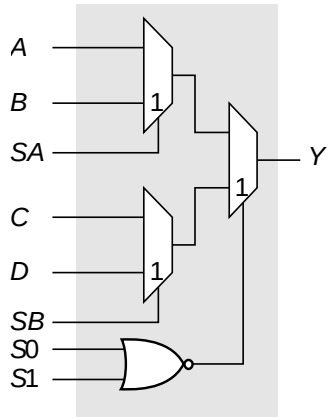


2-input mux as programmable logic block

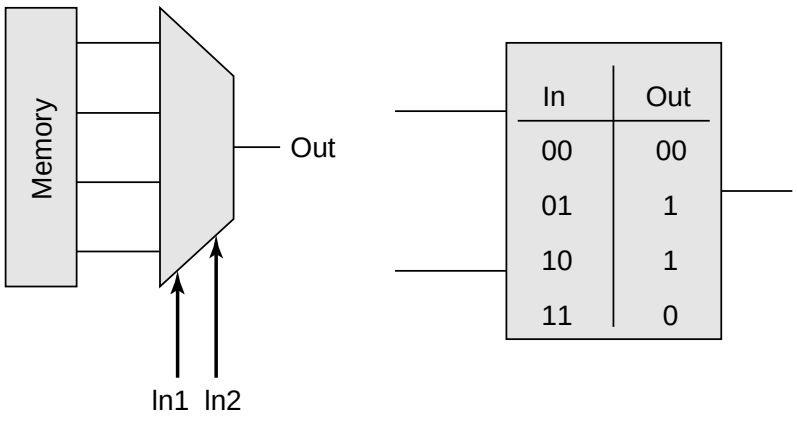


Configuration			
A	B	S	F=
0	0	0	0
0	X	1	X
0	Y	1	Y
0	Y	X	XY
X	0	Y	$X\overline{Y}$
Y	0	X	$\overline{X}Y$
Y	1	X	X 1 Y
1	0	X	$\overline{X}$
1	0	Y	$\overline{Y}$
1	1	1	1

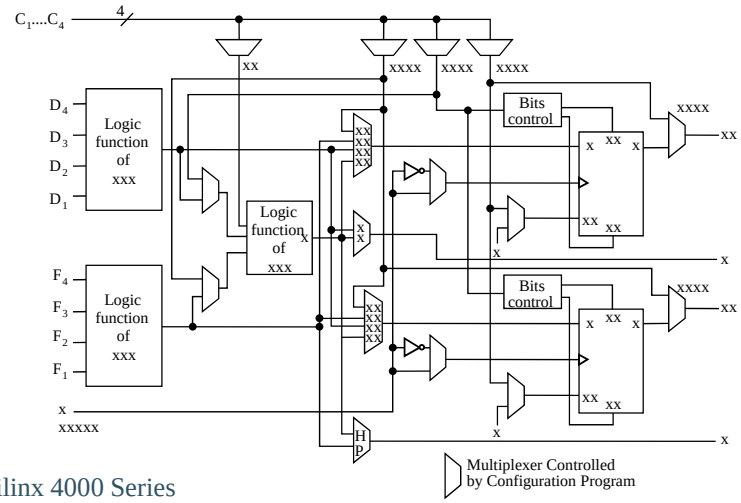
Logic Cell of Actel Fuse-Based FPGA



Look-up Table Based Logic Cell



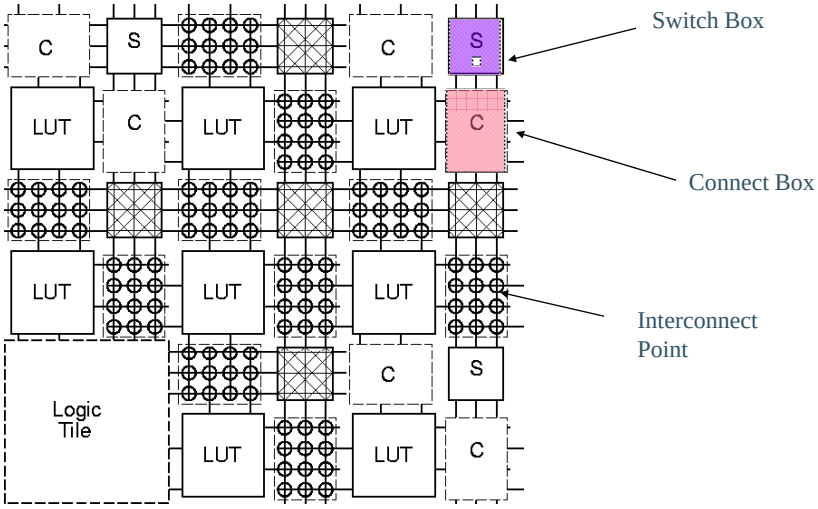
LUT-Based Logic Cell



Xilinx 4000 Series

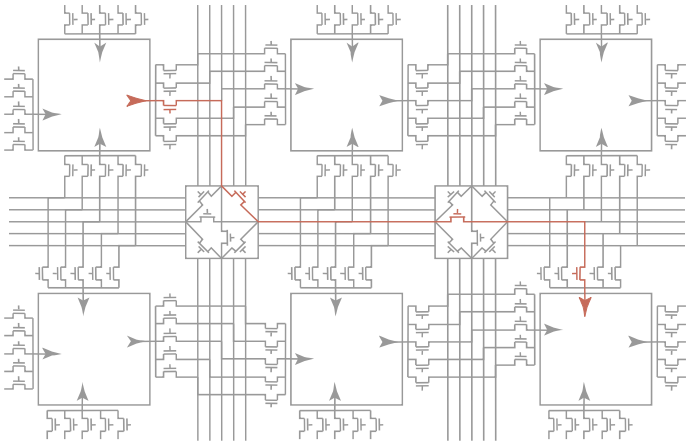
Courtesy Xilinx

Mesh-based Interconnect Network



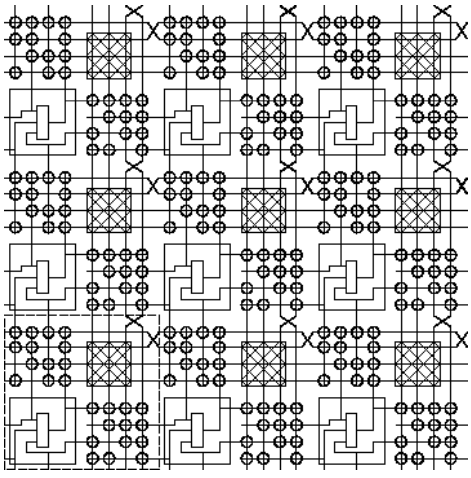
Courtesy Dehon and Wawrzyniek

Transistor Implementation of Mesh



Courtesy Dehon and Wawrzyniek

Hierarchical Mesh Network

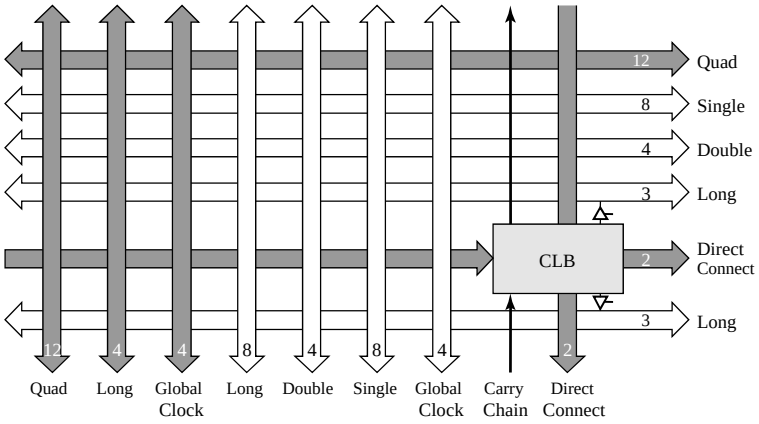


Use overlayed mesh
to support longer connections

Reduced fanout and reduced resistance

Courtesy Dehon and Wawrzyniek

Xilinx 4000 Interconnect Architecture



Courtesy Xilinx