EECS 427

Lecture 3: CMOS review

Reading: 5.4, 6.2

Logistics

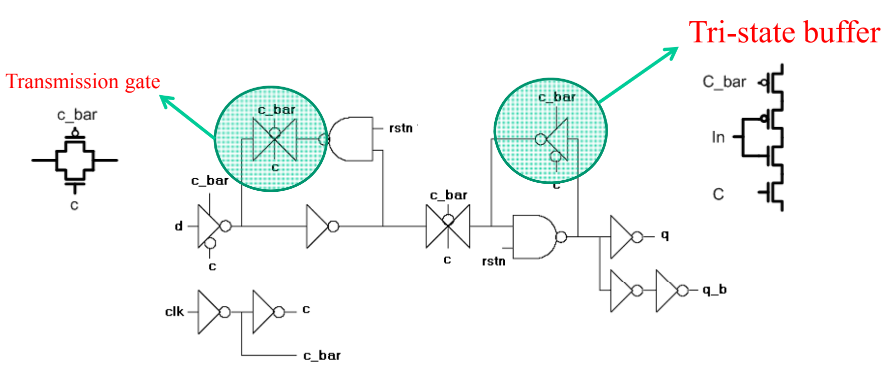
- CAD1 due today at 7pm
- CAD2 assigned yesterday, due next Monday (9/21) at 7pm
- HW1 due next Wednesday (9/23) at the beginning of lecture
- HW1 readings: 3.5, 12.2, 5.4, 6.2.3
- HW2 due in 1.5 weeks
  - Email zhengya at eecs.umich.edu, subject line [EECS427 Project Group]: 1 email per group, include background of each person: grad/undergrad, area of interest/specialty: circuits, architecture, …
  - Good to mix EE and CE, grad and undergrad, foreign and domestic, male and female

Outline

- Last time: layouts and design rules

- Register design for CAD2
- CMOS inverter
- DC and dynamic operations
- Propagation delay
- Static CMOS gates
- Fast gates design techniques

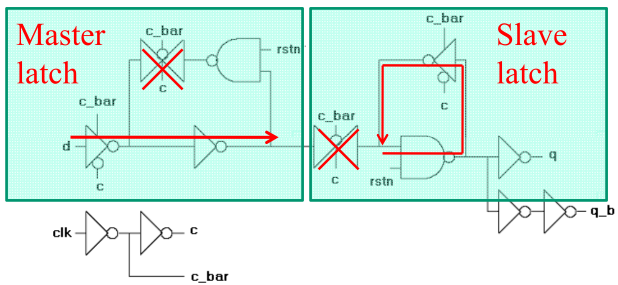
Register Design



Register Design

- How it works

When C is equal to 0, the master latch is transparent, and the salve latch is closed.

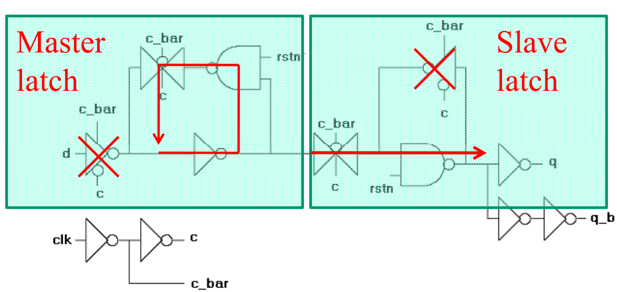


Register Design

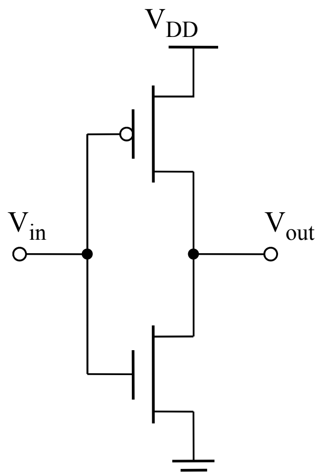
- How it works

When C is equal to 1, the master latch is closed, and the salve latch is transparent

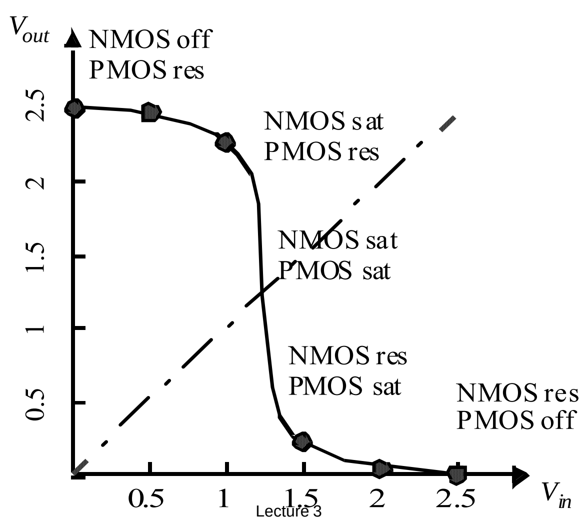
When C switches from 0->1 (rising edge of the clock) the register captures the data .



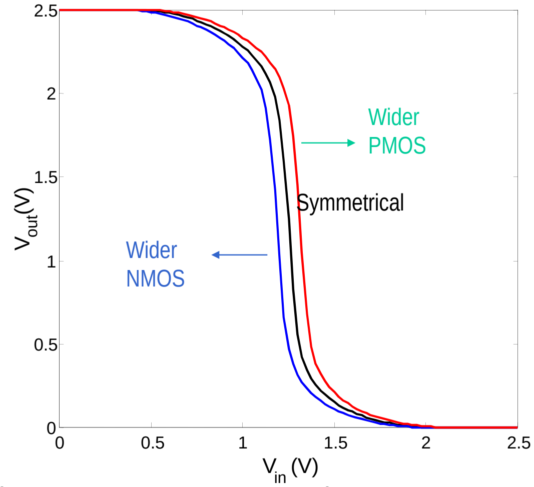
The CMOS Inverter



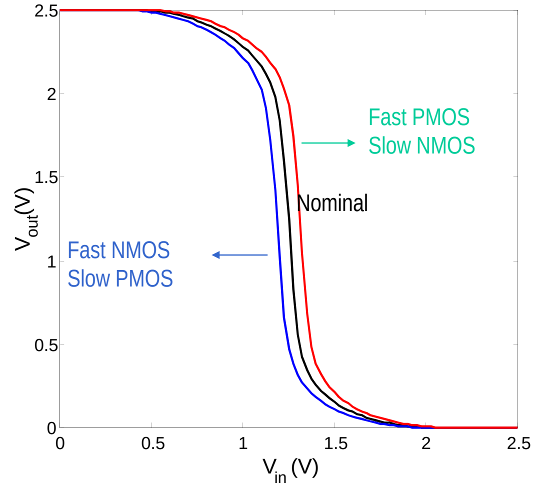
CMOS Inverter VTC



Impact of Sizing

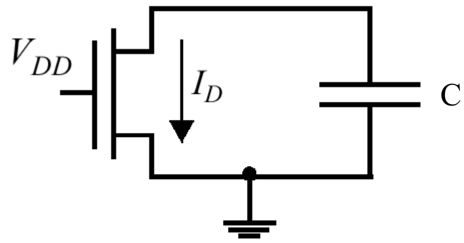


Impact of Process Variation

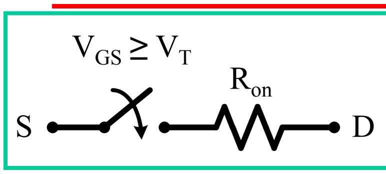


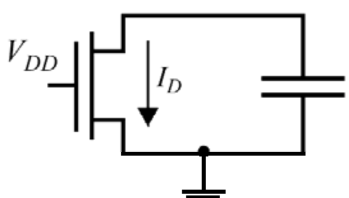
MOS Transistor as a Switch

Discharging a capacitor

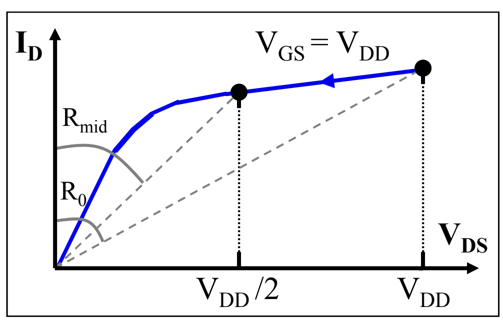


MOS Transistor as a Switch





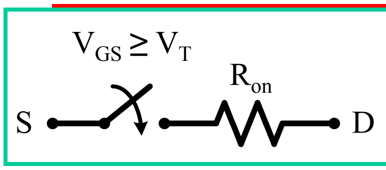
Traversed path

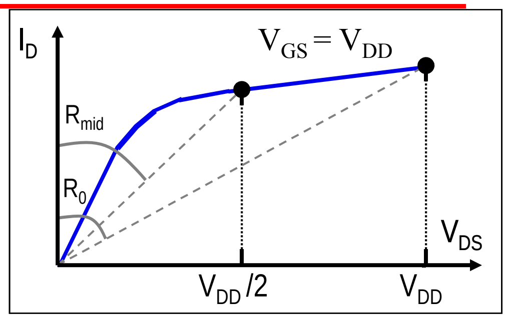


$$R_{eq} = avg(R_{on}(t))\big|_{t=t_1}^{t_2} = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} R_{on}(t)\cdot dt = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)}\cdot dt$$

$$R_{eq} \approx \frac{1}{2}\cdot\left(R_{on}(t_1) + R_{on}(t_2)\right)$$

MOS Transistor as a Switch



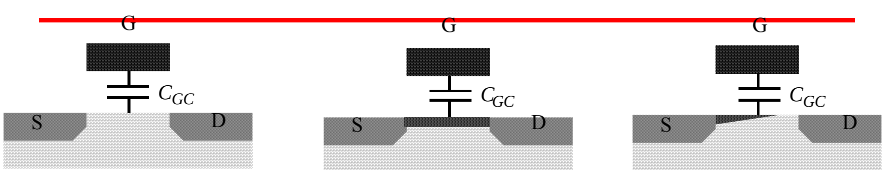


$$R_{eq} = \frac{1}{2} \cdot (R_0 + R_{mid})$$

$$R_{eq} = \frac{1}{2} \cdot \left(\frac{V_{DD}}{I_{DSAT} \cdot (1 + \lambda \cdot V_{DD})} + \frac{V_{DD}/2}{I_{DSAT} \cdot (1 + \lambda \cdot V_{DD}/2)} \right)$$

$$R_{eq} \approx \frac{3}{4} \cdot \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6} \cdot \lambda \cdot V_{DD} \right)$$

Gate-Channel Capacitance



Cut-off Resistive Saturation

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

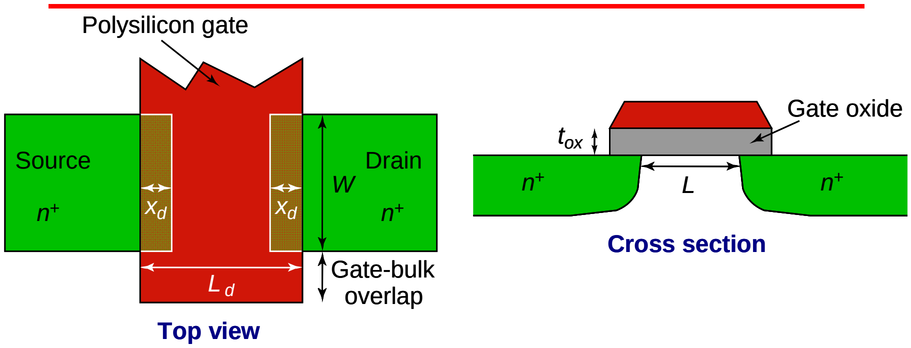
Textbook: page 109

Off/Lin → $C_{gate} = C_{ox} \cdot W \cdot L_{eff}$

Sat → $C_{gate} = (2/3) \cdot C_{ox} \cdot W \cdot L_{eff}$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

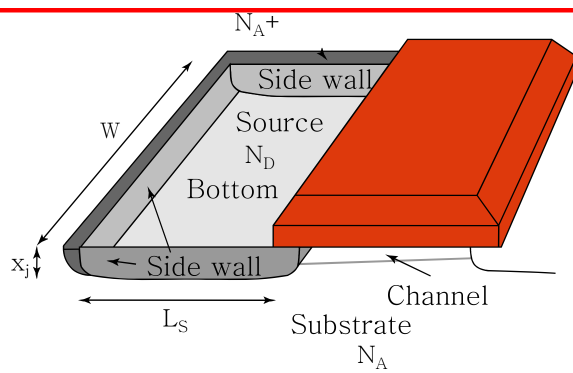
Gate Overlap Capacitance



$$C_O = C_{ox} \cdot x_d$$

Off/Lin/Sat → $C_{GSO} = C_{GDO} = C_O \cdot W$

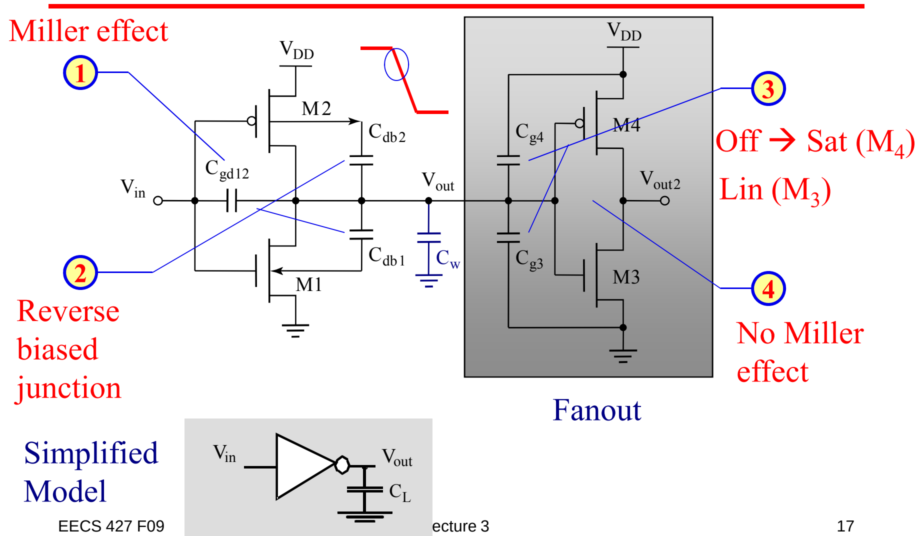
Diffusion Capacitance



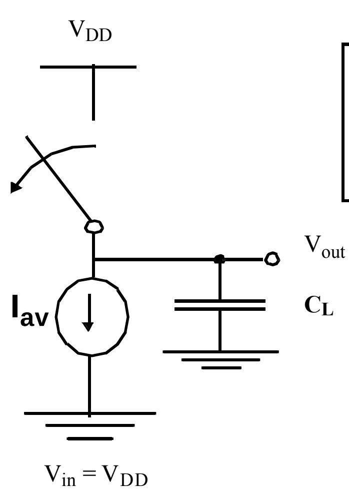
$$C_{diff} = C_{bottom} + C_{sw}$$
$$= C_j \cdot AREA + C_{jsw} \cdot PERIMETER$$

Off/Lin/Sat → $C_{diff} = C_j \cdot L_S \cdot W + C_{jsw} \cdot (2L_S + W)$

Computing the Capacitances



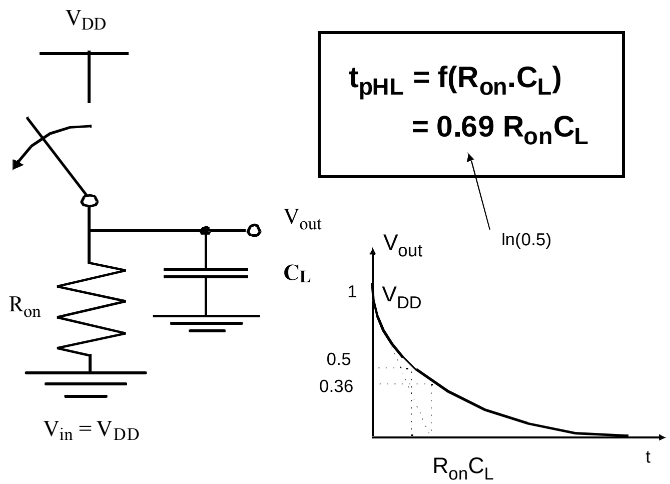
Propagation Delay (Approach 1)



$$t_{pHL} = \frac{C_L\, V_{swing}/2}{I_{av}}$$

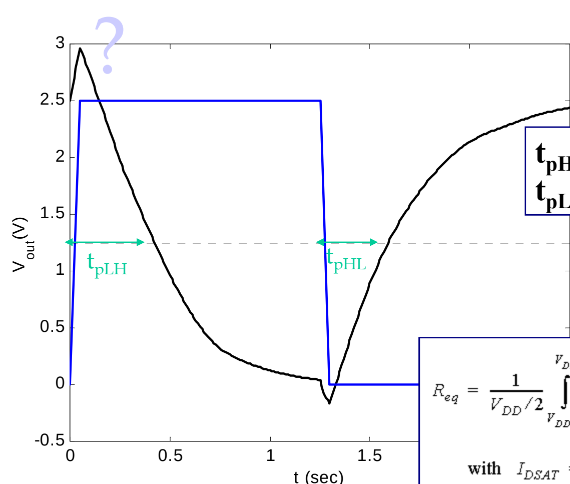
$$\sim \frac{C_L}{k_n\, V_{DD}}$$

Propagation Delay (Approach 2)



$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

Transient Response

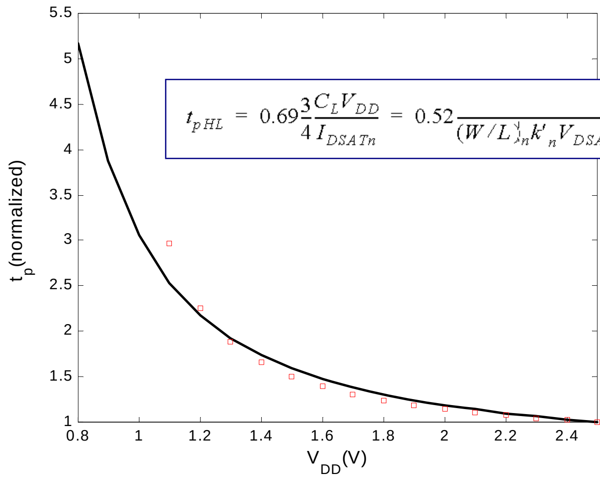


$t_{pHL} = 0.69\ C_L\ R_{eqn}$
$t_{pLH} = 0.69\ C_L\ R_{eqp}$

$$R_{eq} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

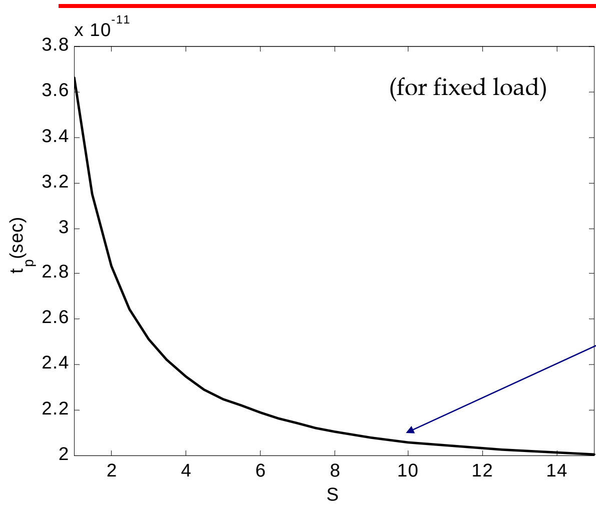
with $I_{DSAT} = k'\frac{W}{L}\left((V_{DD}-V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right)$

Delay as a Function of VDD



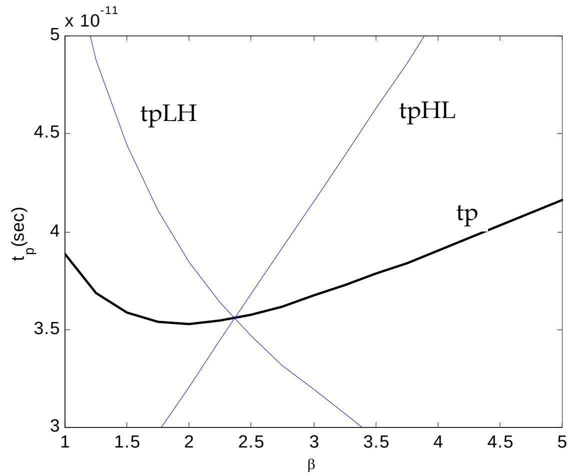
$$t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}} = 0.52\frac{C_L V_{DD}}{(W/L)_n k'_n V_{DSATn}(V_{DD} - V_{Tn} - V_{DSATn}/2)}$$

Device Sizing



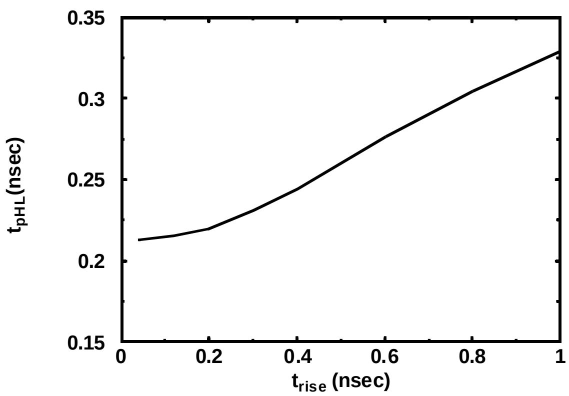
Self-loading effect:
Intrinsic capacitances
dominate

PMOS/NMOS Ratio



$\beta = W_p/W_n$

Input Rise Time



$t_p = t_{step(i)} + \eta t_{step(i-1)}$

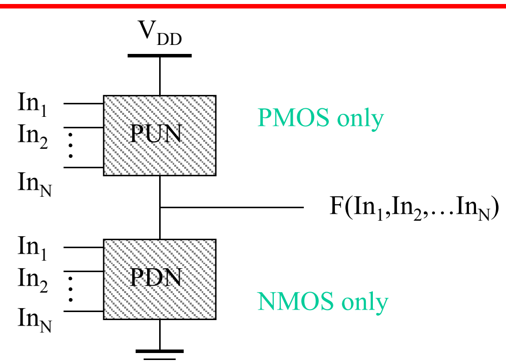
Static CMOS Circuits

At every point in time (except during the switching transients) each gate output is connected to either V_{DD} or V_{SS} via a low-resistive path.

The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit (ignoring, once again, the transient effects during switching periods).

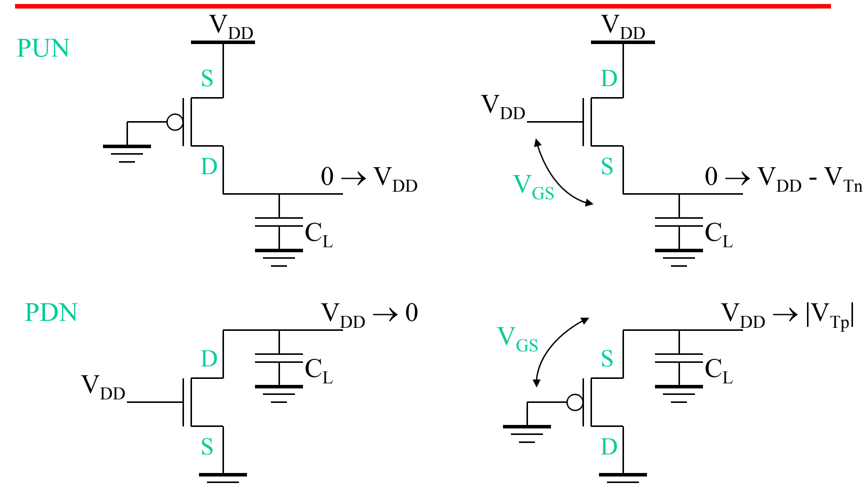
This is in contrast to the dynamic circuit style, which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.

Static CMOS



PUN and PDN are dual logic networks
PUN and PDN functions are complementary

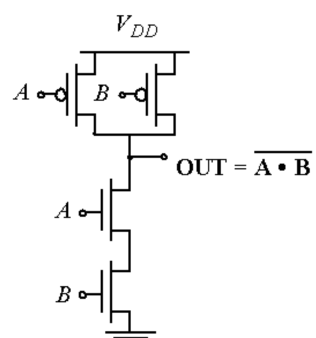
Threshold Drops



NAND Gate

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

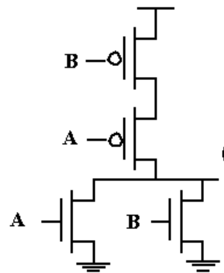


- PDN: $G = AB \Rightarrow$ Conduction to GND
- PUN: $F = \bar{A} + \bar{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}
- $\overline{G(In_1, In_2, In_3, \ldots)} \equiv F(\bar{In_1}, \bar{In_2}, \bar{In_3}, \ldots)$

NOR Gate

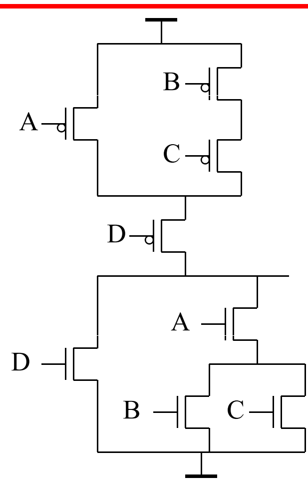
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate



$OUT = \overline{A + B}$

Complex CMOS Gate

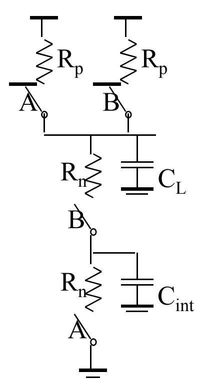


$OUT = \overline{D + A \bullet (B + C)}$

CMOS Properties

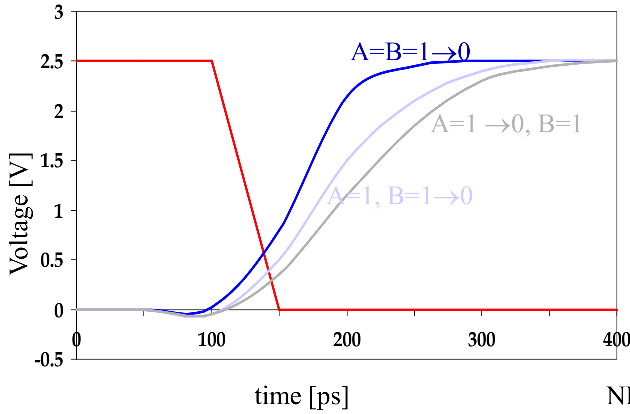
- Full rail-to-rail swing; high noise margins
- Logic levels not dependent upon the relative device sizes; ratioless
- Always a path to Vdd or Gnd in steady state; low output impedance
- Extremely high input resistance; nearly zero steady-state input current
- No direct path steady state between power and ground; no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors

Input Pattern Affects Delay



- Delay is dependent on the pattern of inputs
- Low to high transition
  - both inputs go low
    - delay is 0.69 $R_p/2$ C_L
  - one input goes low
    - delay is 0.69 R_p C_L
- High to low transition
  - both inputs go high
    - delay is 0.69 $2R_n$ C_L

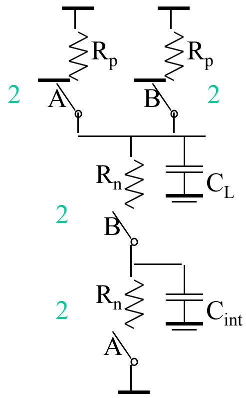
Delay Dependence on Input Patterns

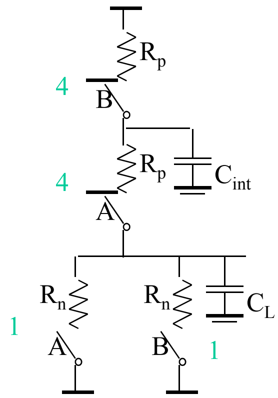


Input Data Pattern	Delay (psec)
A=B=0→1	67
A=1, B=0→1	64
A= 0→1, B=1	61
A=B=1→0	45
A=1, B=1→0	80
A= 1→0, B=1	81

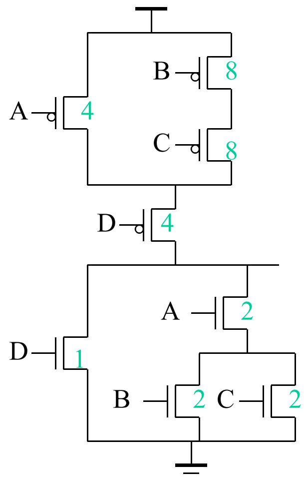
NMOS = 0.5μm/0.25 μm
PMOS = 0.75μm/0.25 μm
C_L = 100 fF

Transistor Sizing



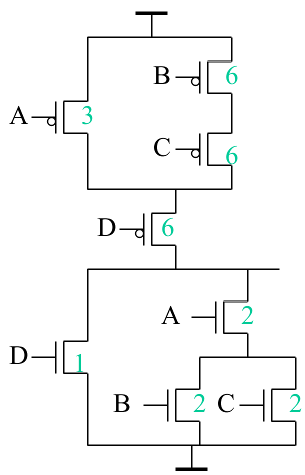


Transistor Sizing



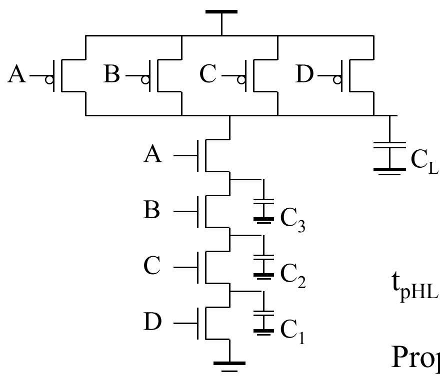
$OUT = \overline{D + A \bullet (B + C)}$

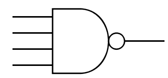
Transistor Sizing



$OUT = \overline{D + A \bullet (B + C)}$

Fan-In Considerations





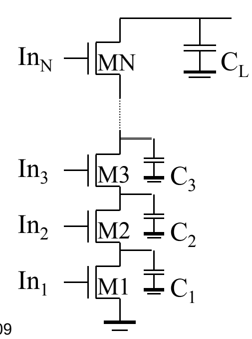
Distributed RC model
(Elmore delay)

$t_{pHL} = 0.69\ R_{eqn}(C_1+2C_2+3C_3+4C_L)$

Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case.

Fast Gates Design Technique

- Transistor sizing
  - as long as fan-out capacitance dominates
- Progressive sizing



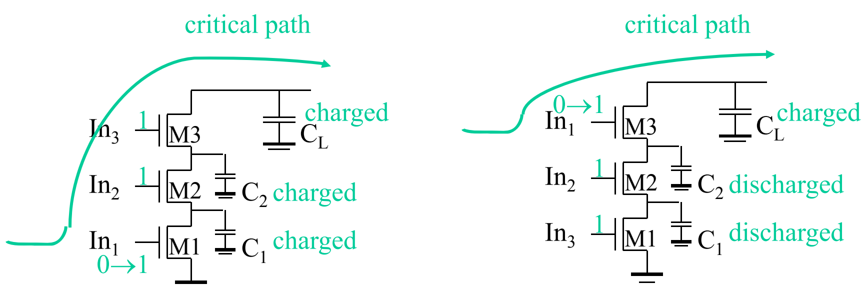
Distributed RC line

M1 > M2 > M3 > … > MN
(the FET closest to the output is the smallest)

Can reduce delay by more than 20%;
Be careful: input loading, junction caps, decreasing gains as technology shrinks

Fast Gates Design Technique

- Transistor ordering



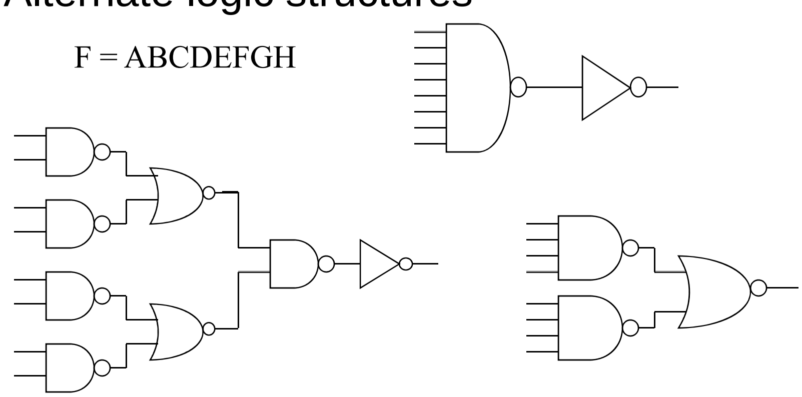
delay determined by time to discharge C_L, C_1 and C_2

delay determined by time to discharge C_L

Fast Gates Design Technique

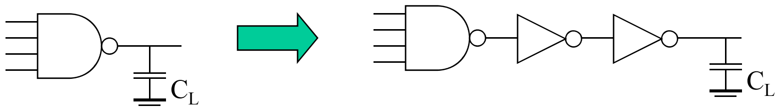
- Alternate logic structures

F = ABCDEFGH



Fast Gates Design Technique

- Isolating fan-in from fan-out using buffer insertion



Fast Gates Design Technique

- Reducing the voltage swing

$$t_{pHL} = 0.69\ (3/4\ (C_L\ V_{DD})/\ I_{DSATn})$$

$$= 0.69\ (3/4\ (C_L\ V_{swing})/\ I_{DSATn})$$

  – linear reduction in delay
  – also reduces power consumption
- But the following gate is much slower!
- Or requires use of “sense amplifiers” on the receiving end to restore the signal level (memory design)

Summary

- CMOS is the dominant circuit family due to:
  - No static power consumption
  - Ease of design
  - Robust to variations and noise

- CAD2 due next Monday at 7 pm
- HW1 due next Wednesday at 1:30 pm
- Form a group. Email zhengya at eecs.umich.edu