Logistics

- CAD1 due today at 7pm
- CAD2 assigned yesterday, due next Monday (9/21) at 7pm
- HW1 due next Wednesday (9/23) at the beginning of lecture
- HW1 readings: 3.5, 12.2, 5.4, 6.2.3
- HW2 due in 1.5 weeks
  - Email zhengya at eecs.umich.edu, subject line [EECS427 Project Group]: 1 email per group, include background of each person: grad/undergrad, area of interest/specialty: circuits, architecture, …
  - Good to mix EE and CE, grad and undergrad, foreign and domestic, male and female
Outline

• Last time: layouts and design rules
• Register design for CAD2
• CMOS inverter
• DC and dynamic operations
• Propagation delay
• Static CMOS gates
• Fast gates design techniques

Register Design

Transmission gate

Tri-state buffer
Register Design

• How it works

When C is equal to 0, the master latch is transparent, and the slave latch is closed.

When C is equal to 1, the master latch is closed, and the slave latch is transparent.

When C switches from 0 to 1 (rising edge of the clock) the register captures the data.
The CMOS Inverter

![CMOS Inverter Diagram]

CMOS Inverter VTC

![CMOS Inverter VTC Graph]
Impact of Sizing

Impact of Process Variation
MOS Transistor as a Switch

Discharging a capacitor

\[ V_{DD} \]
\[ I_D \]
\[ C \]

\[ V_{GS} \geq V_T \]

\[ R_{on} \]

\[ V_{DD} \]

\[ I_D \]

\[ V_{GS} = V_{DD} \]

\[ R_{mid} \]

\[ R_{on} \]

\[ I_D \]

\[ V_{DD}/2 \]

\[ V_{DD} \]

\[ V_{DS} \]

\[ R_{eq} = \text{avg}(R_{on}(t))_{t=t_1}^{t_2} = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} R_{on}(t) \cdot dt \]

\[ R_{eq} \approx \frac{1}{2} \cdot (R_{on}(t_1) + R_{on}(t_2)) \]
MOS Transistor as a Switch

\[ V_{GS} \geq V_T \]

\[ R_{eq} = \frac{1}{2} \cdot (R_0 + R_{mid}) \]

\[ R_{eq} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSAT} \cdot (1 + \lambda \cdot V_{DD})} + \frac{V_{DD}/2}{I_{DSAT} \cdot (1 + \lambda \cdot V_{DD}/2)} \right) \]

\[ R_{eq} \approx \frac{3}{4} \cdot \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{5}{6} \cdot \lambda \cdot V_{DD} \right) \]

Gate-Channel Capacitance

\[ C_{GCB} \]

\[ C_{GCS} \]

\[ C_{GCD} \]

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>( C_{GCB} )</th>
<th>( C_{GCS} )</th>
<th>( C_{GCD} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>( C_{ox} W_{eff} )</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Triode</td>
<td>0</td>
<td>( C_{ox} W_{eff} )</td>
<td>( C_{ox} W_{eff} )</td>
</tr>
<tr>
<td>Saturation</td>
<td>0</td>
<td>( (2/3) C_{ox} W_{eff} )</td>
<td>0</td>
</tr>
</tbody>
</table>

Off/Lin → \( C_{gate} = C_{ox} \cdot W \cdot L_{eff} \)

Sat → \( C_{gate} = (2/3) \cdot C_{ox} \cdot W \cdot L_{eff} \)

\[ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \]
**Gate Overlap Capacitance**

Polysilicon gate

```
Source
n^+

Drain
n^+

Gate oxide

t_{ox}

Gate-bulk overlap

Cross section

Top view

\begin{align*}
    C_O &= C_{ox} \cdot x_d \\
    \text{Off/Lin/Sat} &\rightarrow C_{GSO} = C_{GDO} = C_O \cdot W
\end{align*}
```

**Diffusion Capacitance**

```
\begin{align*}
    C_{\text{diff}} &= C_{\text{bottom}} + C_{\text{sw}} \\
    &= C_j \cdot \text{AREA} + C_{jsw} \cdot \text{PERIMETER} \\
    \text{Off/Lin/Sat} &\rightarrow C_{\text{diff}} = C_j \cdot L_S \cdot W + C_{jsw} \cdot (2L_S + W)
\end{align*}
```
Computing the Capacitances

1. Miller effect
2. Reverse biased junction
3. Off $\rightarrow$ Sat (M₄)
4. Lin (M₃)

Simplified Model

Fanout

Propagation Delay
(Approach 1)

$t_{pHL} = \frac{C_L \cdot V_{swing}}{2 \cdot I_{av}}$

$\sim \frac{C_L}{k_n \cdot V_D}$
Propagation Delay
(Approach 2)

\[ t_{pHL} = f(R_{on} \cdot C_L) = 0.69 \, R_{on} \cdot C_L \]

 transient response

\[ t_{pHL} = 0.69 \, C_L \, R_{eqn} \]
\[ t_{PLH} = 0.69 \, C_L \, R_{eqp} \]
Delay as a Function of VDD

\[ t_{pH} = 0.69 \frac{3C_iV_{DD}}{4I_{DEATn}} + 0.52 \frac{C_iV_{DD}}{(W/L)_{n}k'_{n}V_{DEATn}(V_{DD} - V_{th} - V_{DEATn}/2)} \]

Device Sizing

Self-loading effect: Intrinsic capacitances dominate

(for fixed load)
PMOS/NMOS Ratio

\[ \beta = \frac{W_p}{W_n} \]

\[ t_p = t_{\text{step}(i)} + \eta t_{\text{step}(i-1)} \]

Input Rise Time
Static CMOS Circuits

At every point in time (except during the switching transients) each gate output is connected to either \( V_{DD} \) or \( V_{SS} \) via a low-resistive path.

The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit (ignoring, once again, the transient effects during switching periods).

This is in contrast to the dynamic circuit style, which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.

Static CMOS

PUN and PDN are dual logic networks
PUN and PDN functions are complementary
Threshold Drops

PUN

\[ V_{DD} \rightarrow 0 \rightarrow V_{DD} \]

\[ V_{GS} \rightarrow 0 \rightarrow V_{DD} - V_{Tn} \]

PDN

\[ V_{DD} \rightarrow 0 \]

\[ V_{GS} \rightarrow V_{DD} \rightarrow |V_{Tn}| \]

NAND Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Truth Table of a 2 input NAND gate

- PDN: G = AB ⇒ Conduction to GND
- PUN: F = A + B = AB ⇒ Conduction to V_{DD}
- G(In_1, In_2, In_3, ...) ≡ F(In_1, In_2, In_3, ...)

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NOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Truth Table of a 2 input NOR gate

OUT = A + B

Complex CMOS Gate

OUT = D + A • (B + C)
CMOS Properties

- Full rail-to-rail swing; high noise margins
- Logic levels not dependent upon the relative device sizes; ratioless
- Always a path to Vdd or Gnd in steady state; low output impedance
- Extremely high input resistance; nearly zero steady-state input current
- No direct path steady state between power and ground; no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors

Input Pattern Affects Delay

- Delay is dependent on the pattern of inputs
- Low to high transition
  - both inputs go low
    • delay is $0.69 \frac{R_p}{2} C_L$
  - one input goes low
    • delay is $0.69 R_p C_L$
- High to low transition
  - both inputs go high
    • delay is $0.69 2R_n C_L$
### Delay Dependence on Input Patterns

<table>
<thead>
<tr>
<th>Input Data Pattern</th>
<th>Delay (psec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A=B=0→1</td>
<td>67</td>
</tr>
<tr>
<td>A=1, B=0→1</td>
<td>64</td>
</tr>
<tr>
<td>A=0→1, B=1</td>
<td>61</td>
</tr>
<tr>
<td>A=B=1→0</td>
<td>45</td>
</tr>
<tr>
<td>A=1, B=1→0</td>
<td>80</td>
</tr>
<tr>
<td>A=1→0, B=1</td>
<td>16 81</td>
</tr>
</tbody>
</table>

NMOS = 0.5\,\mu m/0.25\,\mu m  
PMOS = 0.75\,\mu m/0.25\,\mu m  
C_L = 100\,\text{fF}  

#### Transistor Sizing

??
Transistor Sizing

\[ \text{OUT} = D + A \cdot (B + C) \]

Transistor Sizing

\[ \text{OUT} = D + A \cdot (B + C) \]
Fan-In Considerations

Distributed RC model (Elmore delay)

\[ t_{pHL} = 0.69 \cdot R_{eqn} (C_1 + 2C_2 + 3C_3 + 4C_L) \]

Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case.

Fast Gates Design Technique

- Transistor sizing
  - as long as fan-out capacitance dominates
- Progressive sizing

Distributed RC line

\[ M_1 > M_2 > M_3 > \ldots > M_N \]

(the FET closest to the output is the smallest)

Can reduce delay by more than 20%; Be careful: input loading, junction caps, decreasing gains as technology shrinks
Fast Gates Design Technique

• Transistor ordering

![Diagram of transistor ordering with critical paths and delay determination.]

delay determined by time to discharge $C_L$, $C_1$, and $C_2$

delay determined by time to discharge $C_L$

Fast Gates Design Technique

• Alternate logic structures

$F = ABCDEFGH$
Fast Gates Design Technique

- Isolating fan-in from fan-out using buffer insertion

\[ t_{phL} = 0.69 \left( \frac{3}{4} \frac{C_L V_{DD}}{I_{DSATn}} \right) \]

- Reducing the voltage swing
  \[ = 0.69 \left( \frac{3}{4} \frac{C_L V_{swing}}{I_{DSATn}} \right) \]
  - linear reduction in delay
  - also reduces power consumption
- But the following gate is much slower!
- Or requires use of “sense amplifiers” on the receiving end to restore the signal level (memory design)
Summary

• CMOS is the dominant circuit family due to:
  – No static power consumption
  – Ease of design
  – Robust to variations and noise

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• HW1 due next Wednesday at 1:30 pm
• Form a group. Email zhengya at eecs.umich.edu