# Abstract Editor

(Last updated: Oct. 23, 2008)

## Abstract Editor Tutorial

This tutorial has been created to discuss all of the steps needed to create an abstract Library Exchange Format (LEF) file for custom layouts. This abstract view, or LEF file, contains only the essential layer and geometry information (it usually only includes the metal geometries) needed by a place and route tool. Therefore, in order to use a router to combine custom blocks, each block has to have an abstract view and LEF file generated first, and these files are then input to the routing tool.

The CAD3 register file is used in this tutorial as an example.

### Setup

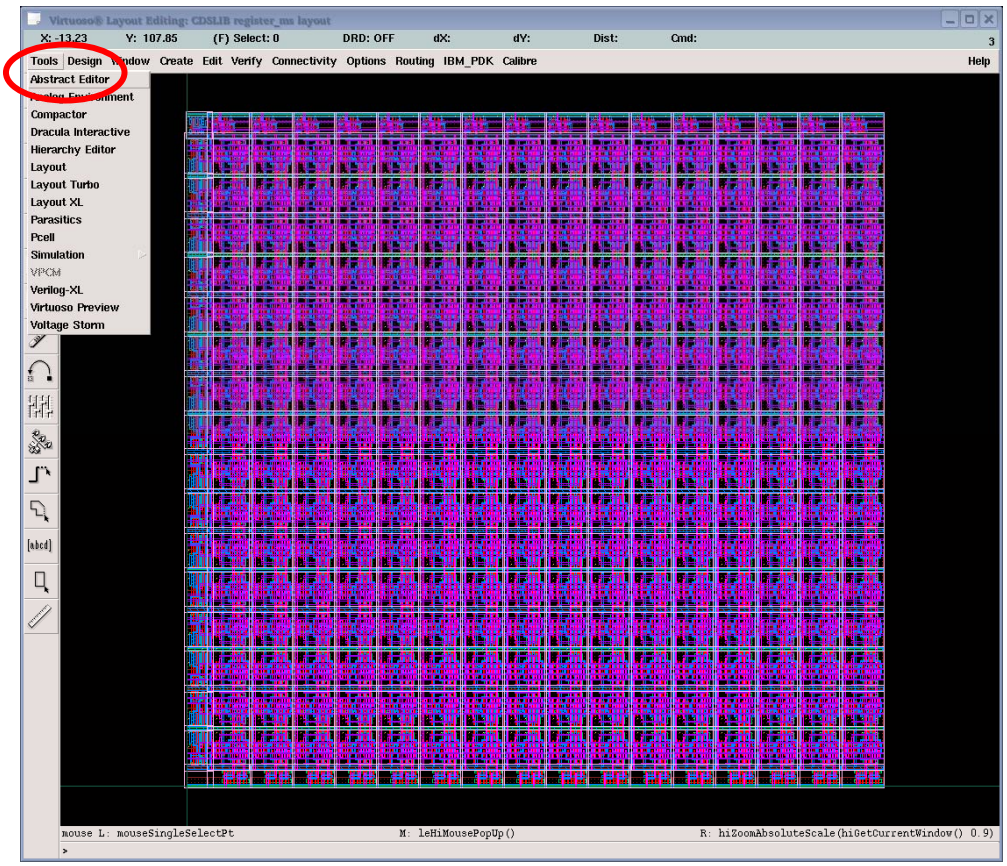
1. Change directories into your **cad3** directory.

   % cd ~/eecs427/cad3

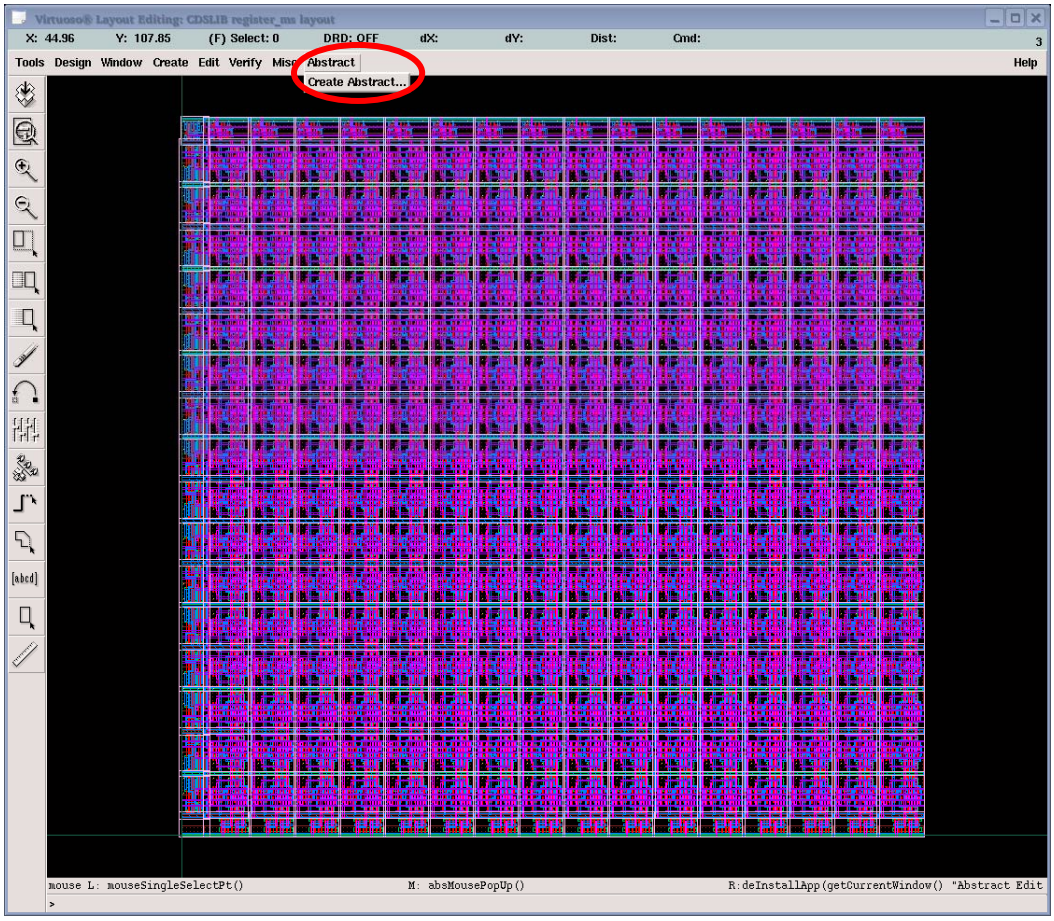
2. Make a new directory called “LEF” in the **cad3** directory.

   % mkdir LEF

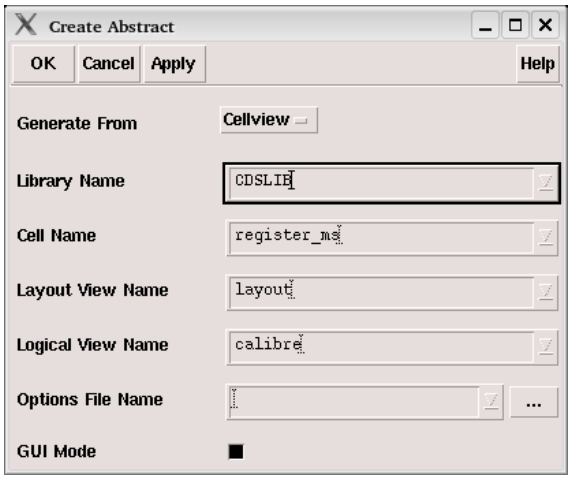
3. Open up ***icfb*** and open the “layout” view of your register file. This will open the Virtuoso Layout Editor.
4. Within Virtuoso, select ***Tools->Abstract Editor***.



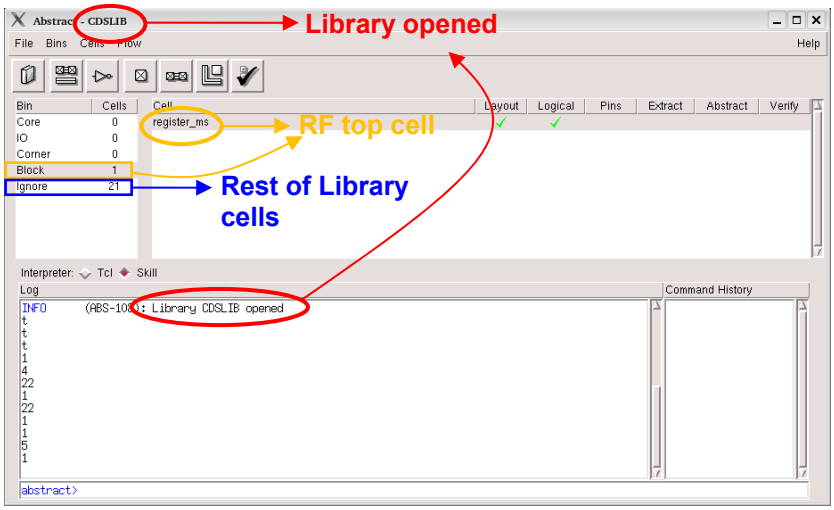
5. You should notice the menus change. The “Connectivity,” “Options,” “Routing,” “IBM_PDK,” and “Calibre” menus are now replaced by “Misc” and “Abstract.”
6. Select ***Abstract->Create Abstract…*** from the newly created abstract window.




7. Next, the “Create Abstract” window will pop-up and the following values should be filled in.

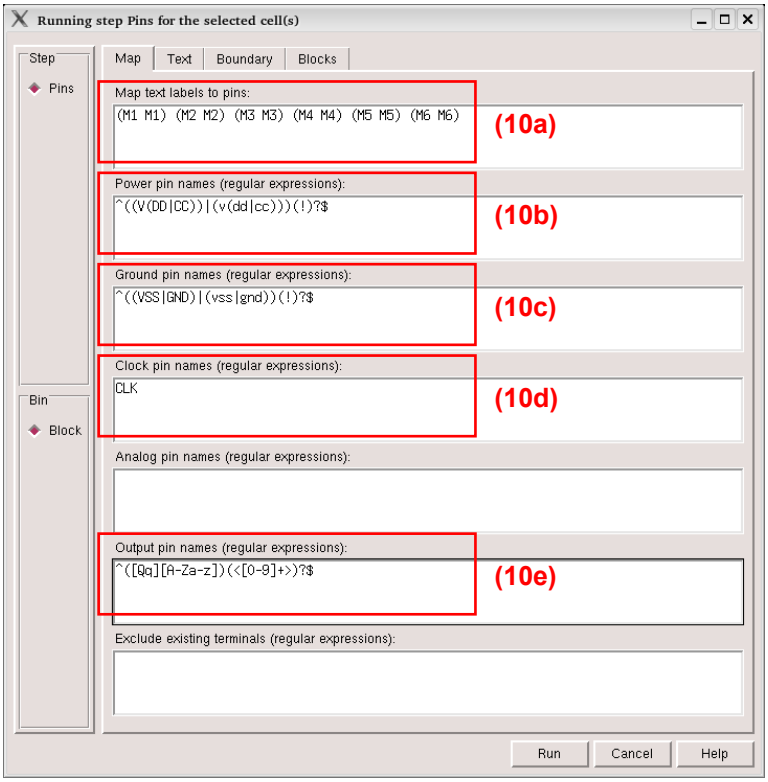



8. Click “OK” and the “Abstract” Window will open. Notice that the cell you just instantiated “Abstract” from is in the “Block” list on the left, while the rest of your libraries files (CDSLIB, in this case) are in the “Ignore” category.

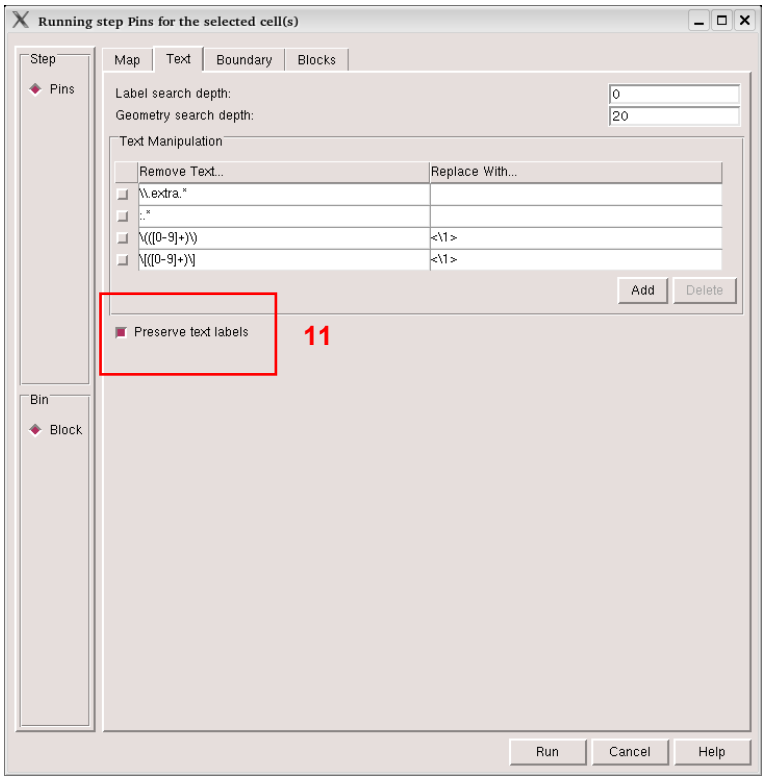



Now we can extract the “abstract” view from the layout of the register file.

9. Click ***Flow->Pins*** in the Abstract window.
10. Fill in the “Map” tab, as shown below.
    a. Tell which text labels to map pins to.
    b. Enter in the power pin names (enter as a regular expression).
    c. Enter in the ground pin names (also as a regular expression).
    d. Enter in the clock pin names (regular expression).
    e. Enter the output pin names (regular expression). In this example, we have output pins named QA, QB, QC, etc. (insensitive to case) which may be followed by a bus bit assignment (e.g., <0>, <1>, etc.). If you do not understand regular expressions, it would be advisable to search online, where there are many regular expression resources and tutorials.

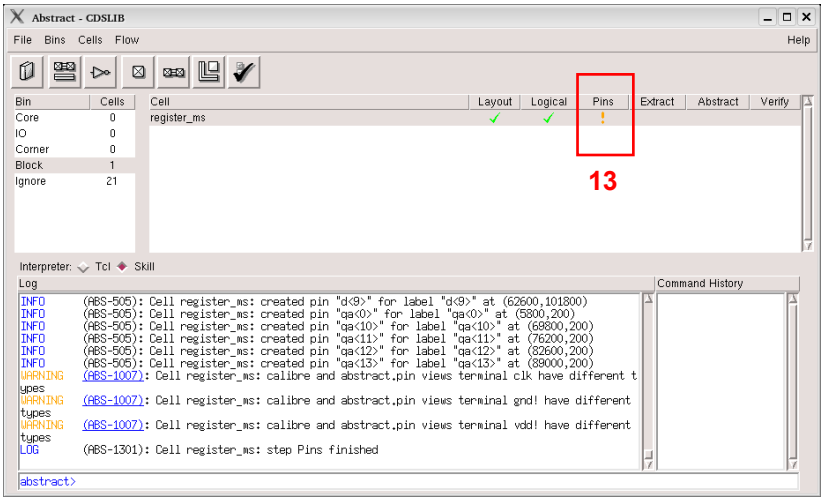


11. Switch to the “Text” tab. Click on the “Preserve text labels” button.



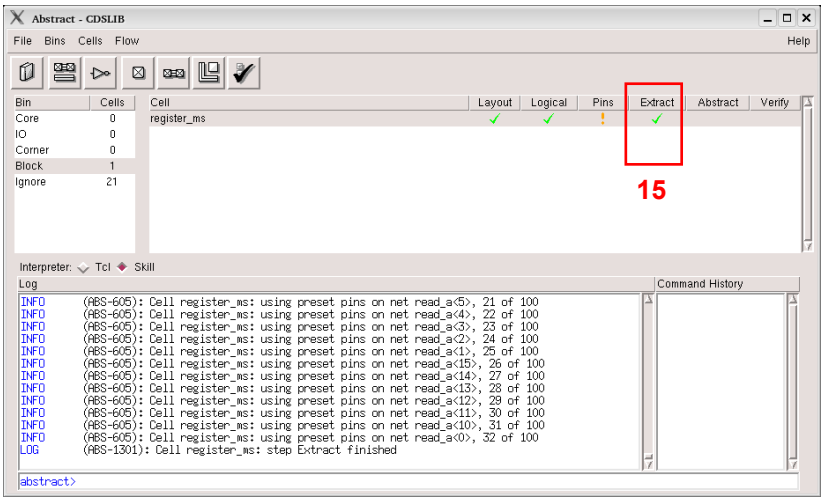

12. Click “Run.” After the run is completed, the “Log” portion of the Abstract window should have a message similar to “Cell register_ms: step Pins finished.” Analyze any WARNINGS and ERRORS that occur in this window. Typically, you can ignore WARNINGS.

13. Once the “Pins” step completes, you should notice that the status of your cell changes. In this example, we had WARNINGS, so a yellow “!” shows up (if you have errors, then a red “x” appears).

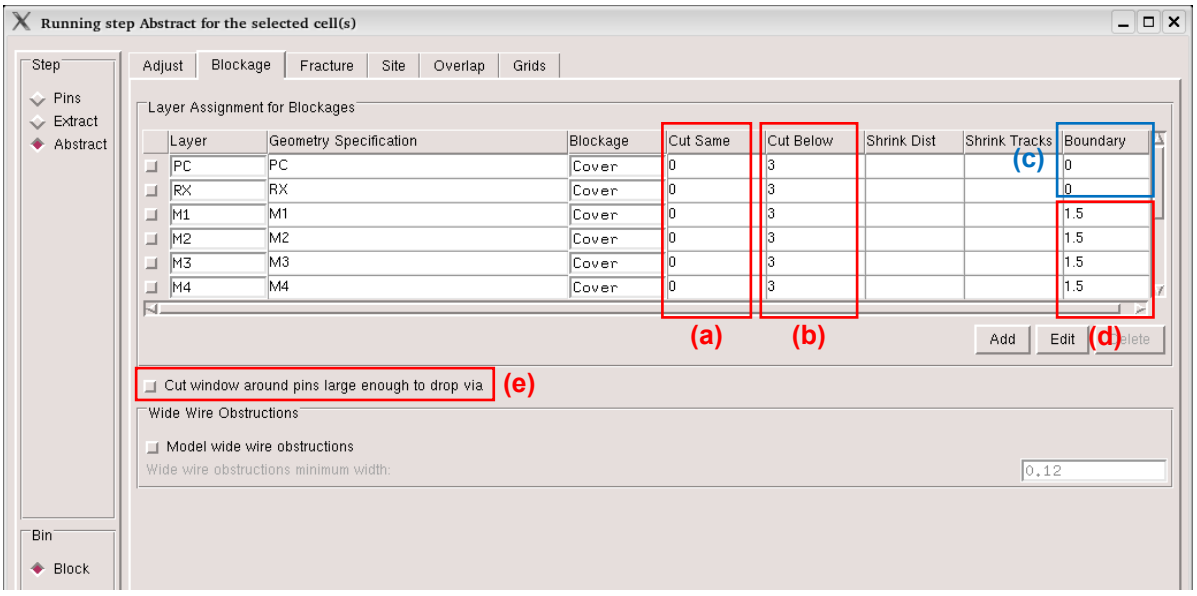



14. Now click ***Flow->Extract***. Then click “Run.”

15. After extraction has completed, there should now be a status in the Abstract window under “Extract.”



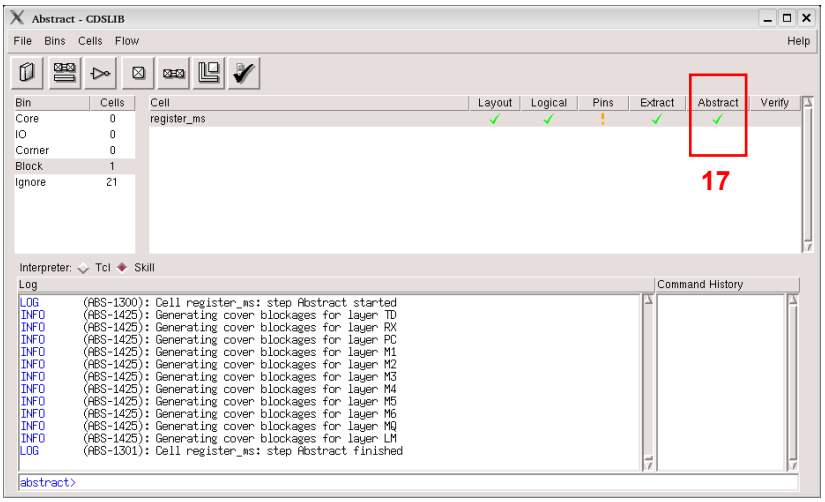

16. Select ***Flow->Abstract***.
17. Fill in the "Blockage" tab (second tab) as described below.
    a. For every layer (PC - TD), enter in "0" (zero) in the "Cut Same" column. This tells Abstract Editor not to cut the blockages around the pin geometries.
    b. For every layer (PC - TD), enter in "3" in the "Cut Below" column. This option puts a 3μm spacing for metal layer blockages over metal pins on the layer below (enabling us to eventually put vias there).
    c. For layers PC and RX, enter in "0" (zero) in the "Boundary" column. This puts PC and RX blockages over the entire block.
    d. For remaining layers (M1 - TD), enter in "1.5" in the "Boundary" column. This puts 1.5μm of space between the prBoundary (place and route boundary) edge and the metal blockage.
    e. Unclick the box "Cut window around pins large enough to drop via." We've already implemented the amount of space we desire in the "Cut Below" column.



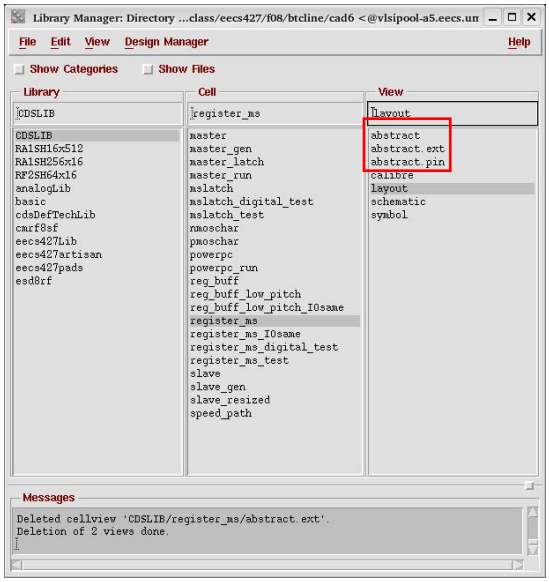

**NOTE: Eventually, we may want to tweak the values that we entered in these columns ("Cut Same," "Cut Below," and "Boundary," depending on whether or not any DRC violations are encountered during place and route.**

18. Click "Run" after you're done making the changes from the previous step.

19. After the abstract generation has completed, there should be a status under “Abstract.”




20. Now there should be 3 new views that appear in your library manager: abstract, abstract.ext, and abstract.pin.




21. Now that you have the abstract view in Cadence, it is time to generate the LEF we will need for placement and routing. Select ***File->Export->LEF*** in the Abstract window. Change the LEF filename and click “OK.” The LEF should now exist and should contain the register file in LEF format.