Exam 1
EECS 427: VLSI Design I
February 19, 2009

Honor Pledge:

I have neither given nor received aid on this examination.

Signature: _____**SOLUTION**_____

IMPORTANT: Underlined text highlights the specific questions you need to answer.

CMOS Manufacturing

1. Given the layout in Figure 1, draw cross-section A-A'. Label the various materials and layers in the cross-section. Also, briefly explain the purpose of the multiple substrate and well contacts serve? Finally, draw the schematic for this layout.
[15 points]

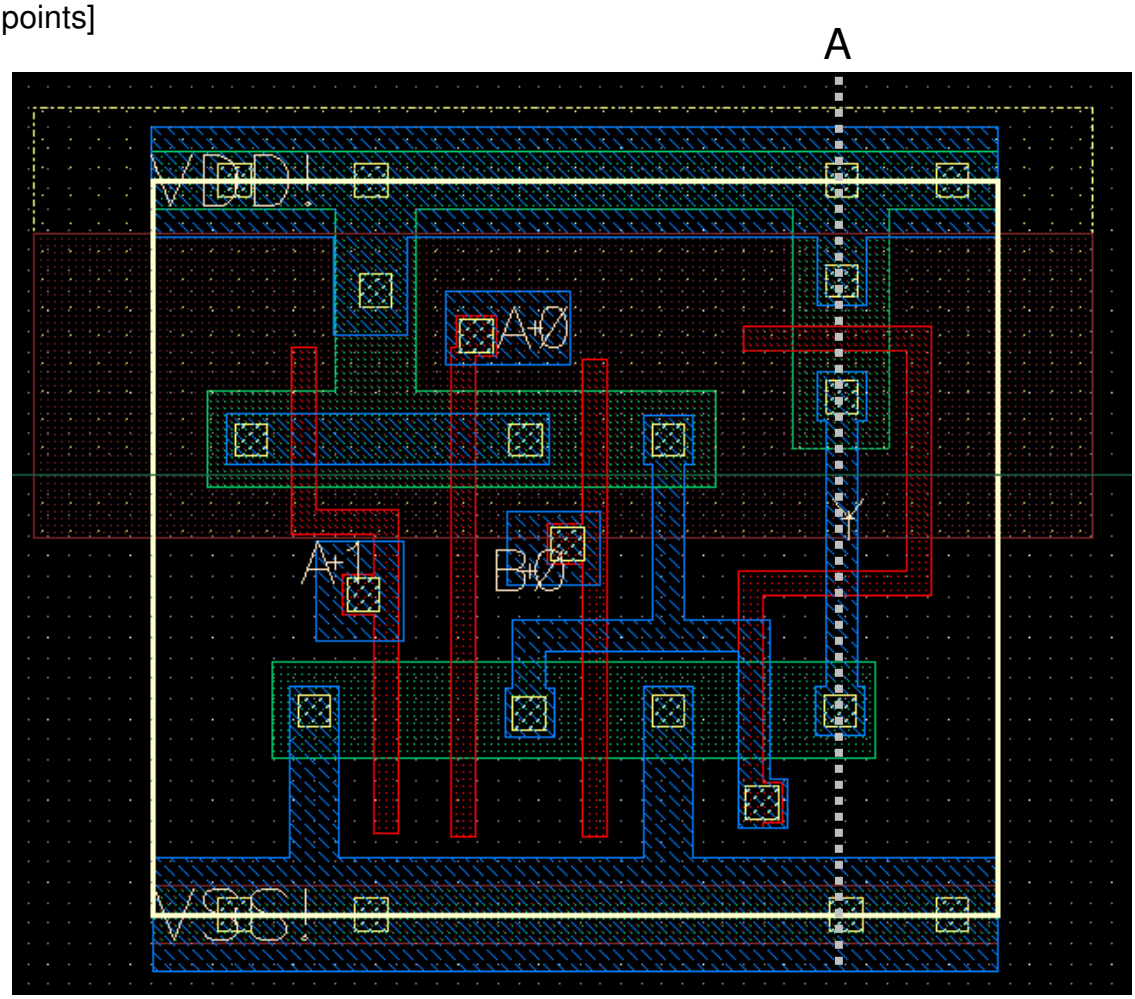
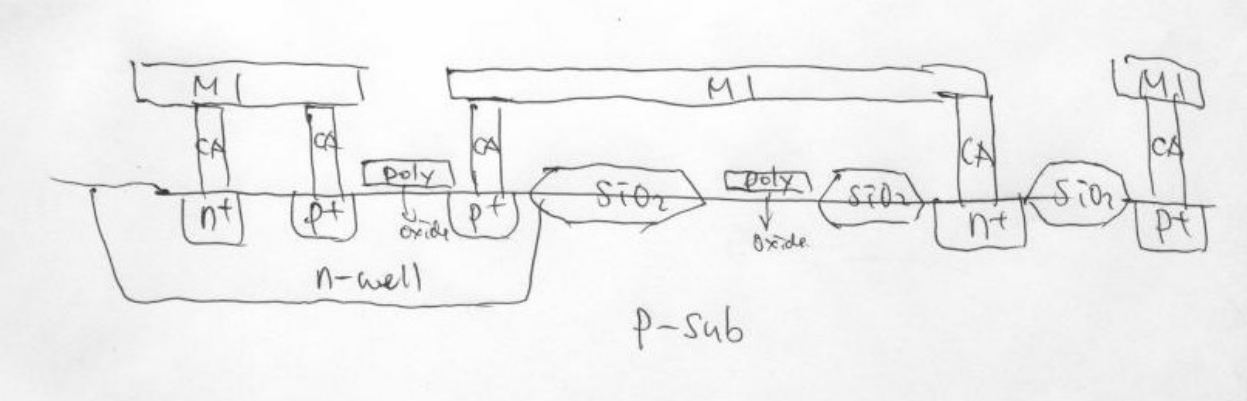
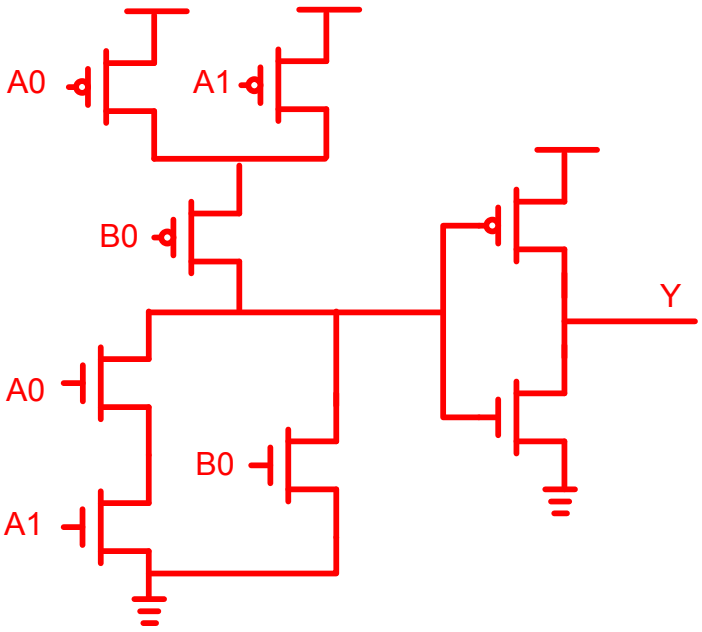


Figure 1

Cross section:



Multiple well and substrate contact help to reduce the distance over which any substrate or well current would flow. By limiting this distance, the path resistance can be reduced and thus, IR drop reduced. This helps suppress latchup, since voltage drops in the substrate often forward bias the PN junction and induce latchup.



Adder Design

2. Consider the 16-bit carry select adder shown in Fig 2. All inputs are initially set to zeros. (T_{MUX}= 200ps, T_{SETUP} = 100ps, T_{SUM}=175ps, T_{CARRY}=100ps for a single bit). [29 points]

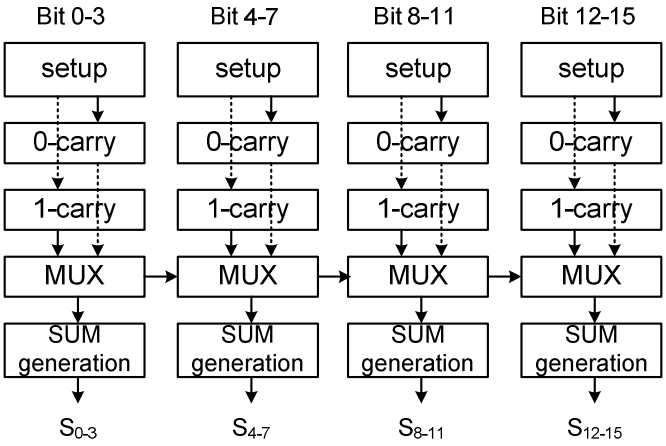


Figure 2

(a) What new input pattern (all inputs arrive simultaneously) results in worst-case delay to the sum, and what is the worst-case delay. [12 points]

LSB MSB

1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

T_{SETUP} + M*T_{CARRY} + N*T_{MUX} + T_{SUM} = 100 + 4*100 + 4*200 + 175 = 1475 ps

(b) Rearrange the carry select adder to achieve minimum delay using block different sizes. How would you partition the adder to achieve minimal delay? [8 points]

T_{MUX} = 200ps = 2*T_{CARRY} (Mux can compensate 2 carry bits)

Possible partitions:
4 groups: 1-3-5-7, delay = 100 + 100 +4*200+ 175 = 1175 ps
3 groups: 3-5-8, delay = 100 + 300 + 3*200 + 100 + 175 = 1275 ps
3-6-7, delay = 100 + 300 + 3*200 + 100 + 175 = 1275 ps

So, 1-3-5-7 is the best.

(c) What is the minimal delay in your new partition? [4 points]

1175 ps

(d) How does the glitch power change after re-partitioning the block sizes (higher/lower/same, with brief explanation)? [5 points]

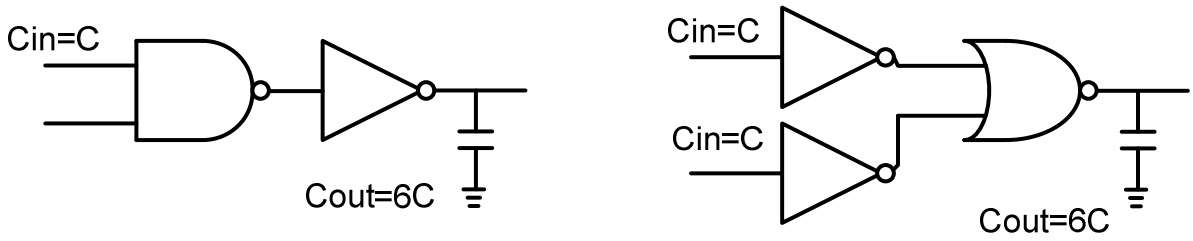
Glitch power is lower after re-partitioning the block size.

When the block size is the same, the MUX select to MSB block will ripple in one block at a time, resulting higher glitch power. However, the new partition balances out the worst case delay of the MUX select controls and the two carry adders, resulting in less glitch power.

Logical Effort

In the following logical effort questions (3-5), assume that a P/N ratio of 1.5 in an inverter results in equal rise and fall delays. The intrinsic delay of an inverter $p_{inv} = 0.6\tau$. See the table at end of this exam for useful information on logical effort.

3. Consider the circuits in Figure 3, both implementing a 2-input AND. What is the path effort of each design? What is the total delay of each design? Which will be faster? Compute the sizes of each logic gate to achieve minimal delay. [14 points]



(a) (b)

Figure 3

$F_{,(a)} = 6 * 7/5 * 1 = 8.4$
$F_{,(b)} = 6 * 1 * 8/5 = 9.6$

$D_{,total,(a)} = 2*(8.4)^0.5 + 0.6 + 2*0.6 = 7.6\ \tau$
$D_{,total,(b)} = 2*(9.6)^0.5 + 0.6 + 2*0.6 = 8\tau$

(a) is faster

Assume 1C per width in µm:

$f_{,(a)} = (8.4)^0.5 = 2.9$, $C_{in,(a),inv} = 6*1/2.9 = 2.07$ C,
$P_{,inv}/N_{,inv} = 1.24$µm / 0.83µm $P_{,nand}/N_{,nand} =$ 0.43µm / 0.57µm

$f_{,(b)} = (9.6)^0.5 = 3.1$, $C_{in,(b),nor} = 6*(8/5)/3.1 = 3.1$ C
$P_{,inv}/N_{,inv} = 0.6$ µm / 0.4µm $P_{,nor}/N_{,nor} =$ 2.325µm / 0.775µm

4. Consider the circuit shown in Figure 4. $C_{in,\,i}$ represents the input gate capacitance, and $C_{wire,i}$ represents the wire capacitance. [18 points]

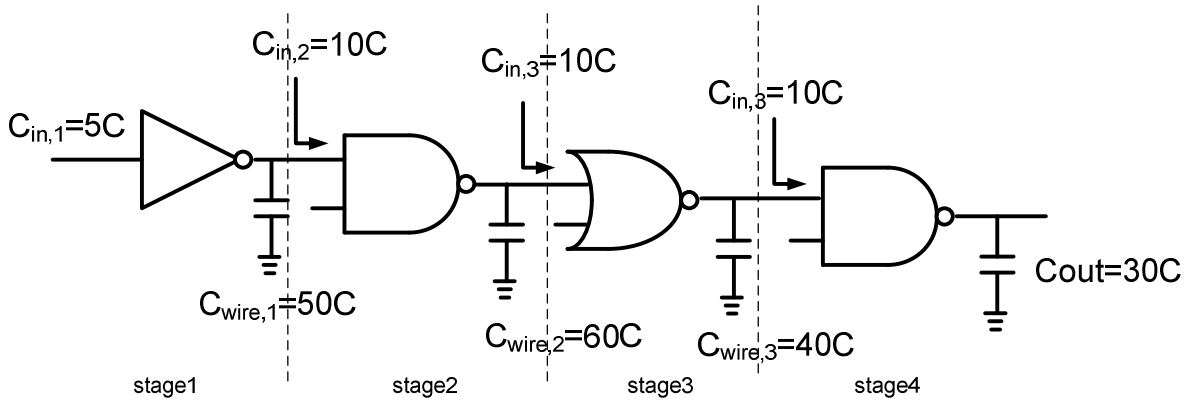


Figure 4

(a) What is the path effort for each stage? What is the total path effort? Do you think 4 is the optimal number of stages? Why? [10 points]

$f_{,s1}$ = 1*12 = 12
$f_{,s2}$ = 7/5*7 = 49/5 = 9.8
$f_{,s3}$ = 8/5*5 = 40/5 = 8
$f_{,s4}$ = 7/5*3 = 21/5=4.2

F = 12 * 9.8 * 8 *4.2 = 3951.36
according to the table, 4 is not the optimal number

(b) Keeping the number of stages fixed at 4 as in Figure 4, now consider sizing up each gate by 2X (including the inverter). What is the new path effort of each stage? What is the total path effort? List two disadvantages of sizing up the gates? [8 points]

$f_{,s1}$ = 1*7 = 7
$f_{,s2}$ = 7/5*4 = 28/5 = 5.8
$f_{,s3}$ = 8/5*3 = 24/5=4.8
$f_{,s4}$ = 7/5*1.5 = 2.1

F = 7 * 5.8 * 4.8 * 2.1 = 409.25

Device size, area, power, larger $C_{in,1}$ to the previous stage.

5. (a) What is the logical effort of the dynamic gate in Figure 5? [6 points]
(Note: size the dynamic gate so that is has the same fall delay as an inverter.)

Logical effort = $C_{in,\ gate}$/ $C_{in,\ inv}$ = 4/5

(b) Use logical effort to explain why dynamic gates perform very well for wide NORs relative to static gates. [6 points]

Logic effort is independent to the number of inputs in dynamic gate.

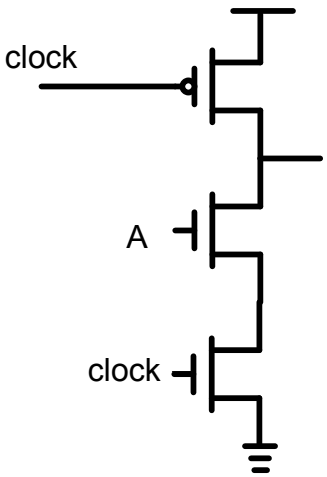


Figure 5

6. Short answer (*be concise*) [12 points]

(a) List two advantages of a modified Booth multiplier compared to a conventional multiplier? [6 points]

2's complement computation and fewer partial products.

(b) How many control bits are needed for a 16-bit $\log_4$ shifter? List the truth table for the shifter (indicate the i_{th} stage control bits, and total shift amount) [6 points]

4 bits, 2bit/stage

Stage 1: shift 0/1/2/3
Stage 2: shift 0/4/8/12

Stage1	Stage2	Shift amount
0 0	0 0	0
0 1	0 0	1
1 0	0 0	2
1 1	0 0	3
0 0	0 1	4
0 1	0 1	5
1 0	0 1	6
1 1	0 0	7
0 0	1 0	8
0 1	1 0	9
1 0	1 0	10
1 1	1 0	11
0 0	1 1	12
0 1	1 1	13
1 0	1 1	14
1 1	1 1	15

Best number of stages for $p_{inv} = 0.6\tau$

Path effort F	Best number of stages $\hat{f}$	Min. delay $\hat{D}$	Stage effort f
0		1.0	
	1		0-5.1
5.13		5.7	
	2		2.3-4.2
17.7		9.6	
	3		2.6-3.9
59.4		13.5	
	4		2.8-3.7
196		17.4	
	5		2.9-3.6
647		21.2	
	6		2.9-3.6
2130		25.1	
	7		3.0-3.5
6980		29.0	

I. Sutherland, *et al*, Logical Effort, Academic Press, 1999