The University of Michigan
Department of Electrical Engineering and Computer Science

EECS 427 Fall 2008

Quiz 2

Name:______________________ UM ID:_________________

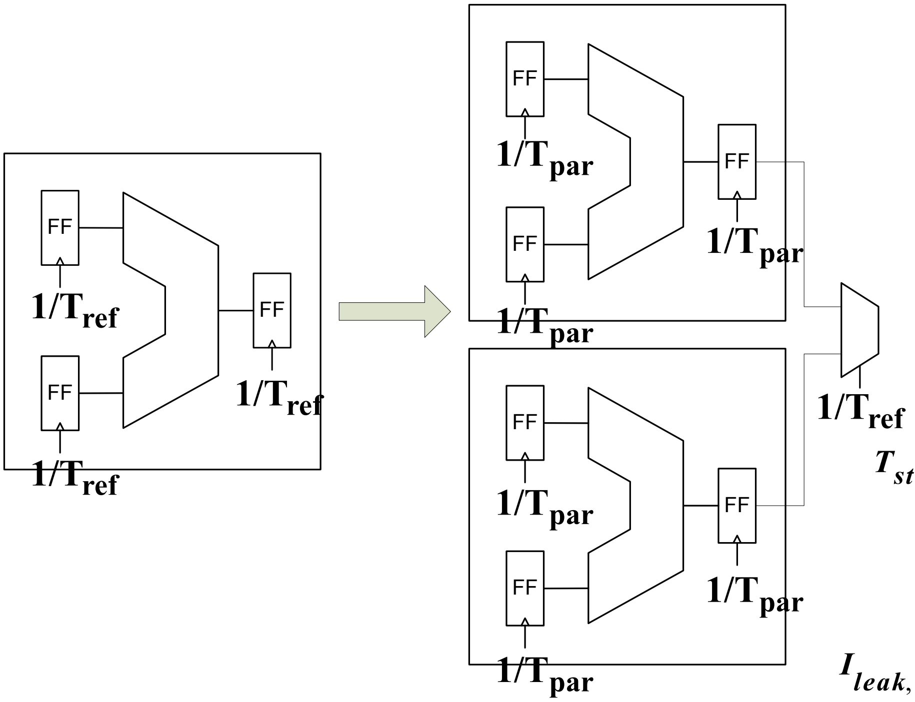
For full credit, show the pertinent work leading to your answers

Problem #	Maximum Possible Points	Points Obtained
1	19	
2	8	
3	13	
4	12	
5	19	
6	6	
7	6	
8	17	
Total	100	

I have neither given nor received any unauthorized aid during this exam

Signed: ____________________________

1.0 Problem 1 (19 Points) – Parallelism



$$T_{stage} = T_0 \frac{V_{DD}}{(V_{DD}-V_{th})^2}$$

$$I_{leak,\,stage} = I_0 e^{\left(\frac{V_{gs}-V_{th}}{nV_T}\right)}$$

(a) Singe Execution Stage (Ref) (b) Parallel Execution Stage (Par) (c) Useful Equations

Figure 1. Circuit for Problem 1.0.

Circuit Parameters: T_0 = 1x10^{-9} s•V$^{0.5}$; $V_{DD,ref}$ = 1.2V; V_{th} = 0.4V; total switching capacitance of one single execution stage, C_{tot} = 200fF; switching activity (avg. # of high-to-low or low-to-high transitions in one clock cycle), α = 0.2; n = 1; V_T = 26mV; C_{mux} = 20fF; I_0 = 60A.

During the early stages of a block design, a designer determines that there are two possible implementations of the circuit, shown in Figure 1a and Figure 1b. The area specifications for the design allow for either a single execution stage (Figure 1a) or a 2-way parallel execution stage (Figure 1b). Both implementations must result in the *same* throughput. **Use the equations shown in Figure 1c in your answers to the following questions.**

1.1 (4 Points) What supply voltage, $V_{DD,par}$, can the 2-way parallel implementation operate at? Ignore the additional delay added by the mux in the 2-way parallel case.

$V_{DD,par}$ = **0.8861V**

(work on next page)

Two-way Parallelism → $T_{par} = 2T_{ref}$

$$T_{par} = T_0\frac{V_{DD,par}}{(V_{DD,par} - V_{th})^2} = 2T_{ref} = 2T_0\frac{V_{DD,ref}}{(V_{DD,ref} - V_{th})^2} = 3.75 \times 10^{-9}$$

$$V_{DD,par} = 3.75 \cdot (V_{DD,par} - V_{th})^2$$

$$3.75V_{DD,par}^2 - 4V_{DD,par} + 0.6 = 0$$

$$\therefore V_{DD,par} = 0.8861\text{V}$$

1.2 (6 Points) What is the gain/loss in total power of the parallel implementation, $P_{total,par}$, relative to the original power, $P_{total,ref}$? Consider both leakage and dynamic power. Ignore the additional leakage added by the mux in the 2-way parallel case.

$$\frac{P_{total,par}}{P_{total,ref}} = 0.869$$

$$f_{ref} = 1 \times 10^{-9} \cdot \frac{1.2}{(1.2 - 0.8)^2} = 533.33\text{MHz}$$

$$P_{dyn,par} = C_{tot,par} \cdot V_{DD,par}^2 \cdot f_{par} \cdot \alpha = (2C_{tot} + C_{mux}) \cdot 0.8861^2 \cdot \frac{1}{2}f_{ref} \cdot 0.2$$

$$= 420\text{fF} \cdot 0.8861^2 \cdot \frac{1}{2}(533.33\text{MHz}) \cdot 0.2 = 17.588\mu\text{W}$$

$$P_{leak,par} = V_{DD,par} \cdot I_{leak,par} = 0.8661 \cdot 2I_{stage} = 0.8661 \cdot 2 \cdot I_0 e^{\frac{V_{gs} - V_{th}}{nV_T}}$$

$$= 0.8661 \cdot 2 \cdot 60 \cdot e^{\frac{-0.4}{1 \cdot 26\times10^{-3}}} = 0.8661 \cdot 120 \cdot 2.082\times10^{-7} = 22.142\mu\text{W}$$

$$\therefore P_{total,par} = 17.588\mu\text{W} + 22.142\mu\text{W} = 39.730\mu\text{W}$$

(continued on next page)

$$P_{dyn,ref} = C_{tot,ref} \cdot V_{DD,ref}^2 \cdot f_{ref} \cdot \alpha = 200\text{fF} \cdot 1.2^2 \cdot 533.33\text{MHz} \cdot 0.2 = 30.720\mu\text{W}$$

$$P_{leak,ref} = V_{DD,ref} \cdot I_{leak,ref} = 1.2 \cdot I_{stage} = 1.2 \cdot I_0 e^{\frac{V_{gs} - V_{th}}{nV_T}}$$

$$= 1.2 \cdot 60 \cdot e^{\frac{-0.4}{1 \cdot 26\times10^{-3}}} = 1.2 \cdot 60 \cdot 2.082\times10^{-7} = 14.993\mu\text{W}$$

$$\therefore P_{total,ref} = 30.720\mu\text{W} + 14.993\mu\text{W} = 45.713\mu\text{W}$$

$$\therefore \frac{P_{total,par}}{P_{total,ref}} = \frac{39.730}{45.713} = 0.869$$

1.3 (5 Points) A designer decides to exploit as much parallelism as possible while maintaining constant throughput. As the number of parallel execution units approach ∞, describe the following **four** quantities:

1. $V_{DD,par\_\infty} =$

$$\frac{V_{DD,par}}{(V_{DD,par} - 0.4)^2} = n \cdot 1.875 \Rightarrow 1.875nV_{DD,par}^2 - (1.5n+1)V_{DD,par} + 0.3n = 0$$

$$V_{DD,par} = \frac{(1.5n+1) \pm \sqrt{3n+1}}{3.75n} \Rightarrow \lim_{n\to\infty} \frac{1.5n}{3.75n} \pm \frac{\sqrt{3n}}{3.75n} = \frac{1.5}{3.75} = 0.4 = \text{constant}$$

2. $$P_{Dyn,par\_\infty} = (nC_{tot} + C_{mux}) \cdot V_{DD,par}^2 \cdot \frac{1}{n} f_{ref}\left(\alpha \Rightarrow \lim_{n\to\infty} nC_{tot} \cdot 0.4^2 \frac{1}{n} f_{ref}\alpha\right) = 0.16C_{tot}f_{ref}\alpha = 3.413\mu\text{W} = \text{const.}$$

3. $$P_{leak,par\_\infty} = V_{DD,par} \cdot nI_{stage} = 0.4 \cdot n \cdot 12.494\mu\text{A} \Rightarrow \lim_{n\to\infty} 0.4 \cdot n \cdot 12.494\mu\text{A} = \infty$$

4. Total power, P_{total,par_∞} relative to P_{ref}. Is it [✓ more,] less, equal (circle one)

Explain. **The supply voltage and, therefore, dynamic power approach a constant value as n → ∞ but leakage power → ∞. Thus, total power also approaches ∞, so it is greater than P_{ref}.**

1.4 (4 Points) Consider a different execution stage than the one described by the parameters in this problem. You find that with this execution stage, a parallelism of 2 has higher power than a parallelism of 1. *List at least three parameters* that could have caused this higher power and *whether these parameters would have been higher or lower than in the original case* in Problem 1.1.

I_0↑, C_{mux}↑, or α↓

2.0 Problem 2 (8 Points) – Dynamic Logic Techniques

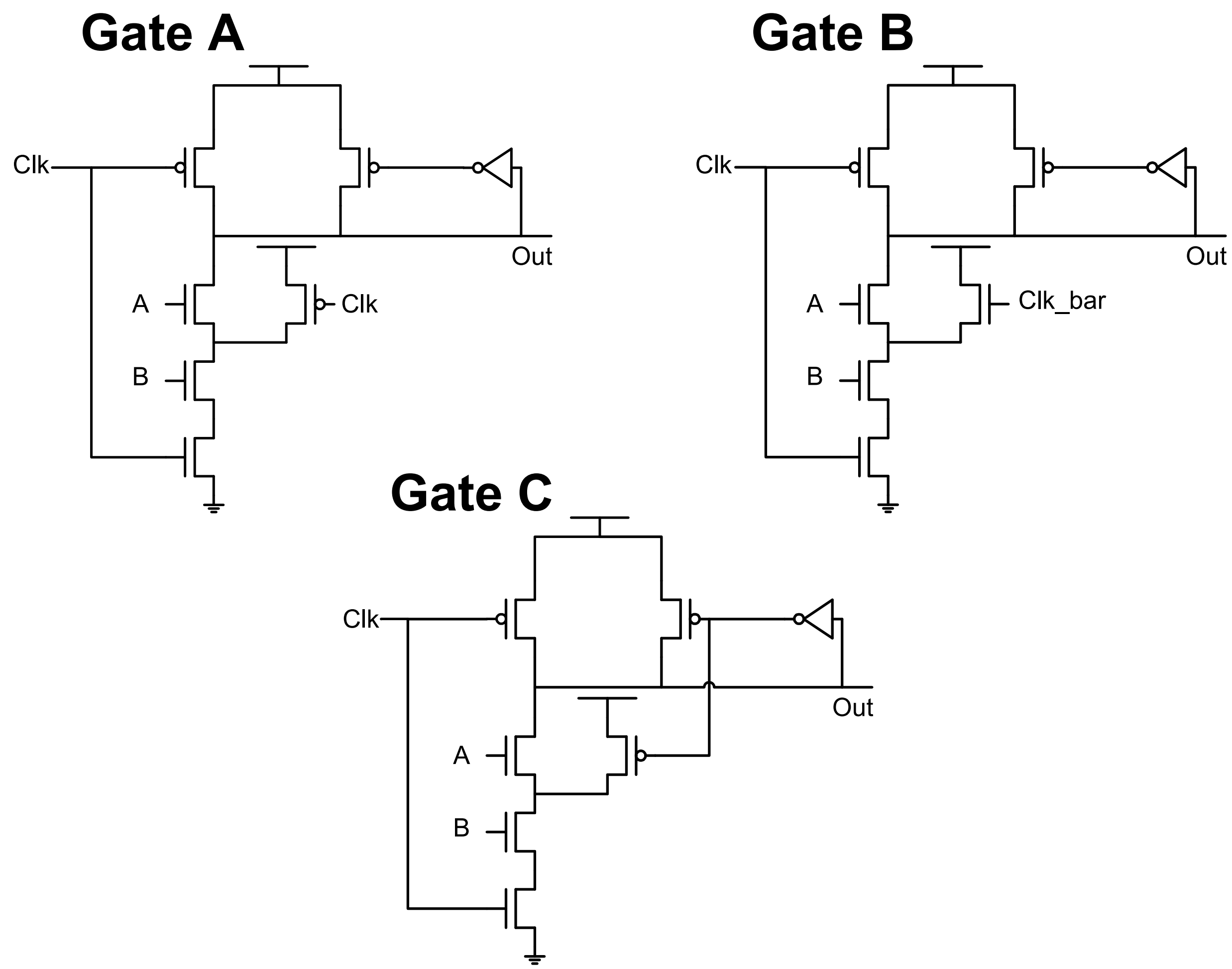


Figure 2. Three dynamic logic gates for Problem 2.0.

Presented are three variations of a dynamic 2-input NAND gate. *Please order them in robustness and speed.* **Explain briefly below.**

SPEED		**ROBUSTNESS**	
Fastest	**B**	Most Robust	**C**
Medium	**A**	Medium	**A**
Slowest	**C**	Least Robust	**B**

Explain: **B is the fastest because the internal node is precharged to Vdd - Vt, as opposed to Vdd in the other cases (so there can be less stored charge to be discharged during evaluate). It is also the least robust because charge-sharing can now have more of an effect (if input A goes high and input B is low, the output node will be pulled down slightly).**

C is both the slowest and most robust because the babysitter acts similar to a second keeper, so there is more contention to the low-going transition, but a 1 at the output is held stronger.

3.0 Problem 3 (13 Points) – Process Variation

Below are two logic cones in the same circuit. Assume that without process variation, all gates have the same delay, and interconnect delays are equal. Also, assume that the only source of variation in gate delay is from variation in threshold voltage, V_{th}. Finally, assume that the AND gates are not affected by variation.

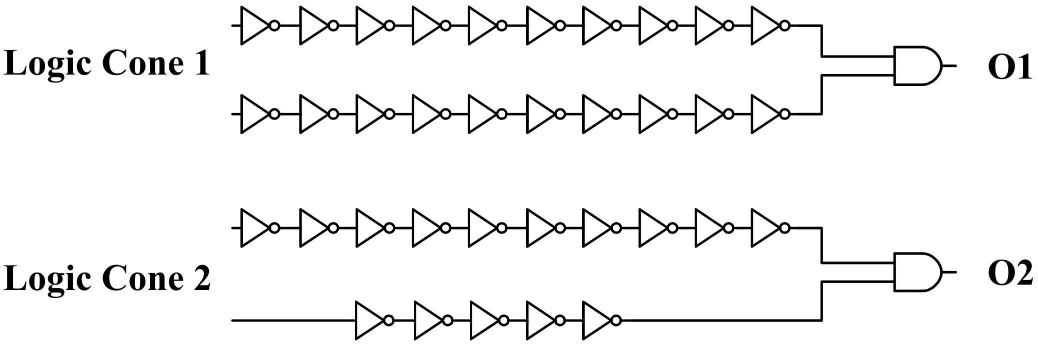


Figure 3. Two logic cones under examination in Problem 3.0.

a) **(4 Points)** If V_{th} **variation is uncorrelated**, which output (O1 or O2) is expected to have worse **99th percentile delay**, or are the 99th percentile delays equal? **Explain.**

Logic Cone 1 will be worse. Since it has two critical paths as opposed to one, there is a greater chance that it has the worst critical path after uncorrelated variation.

b) **(4 Points)** If V_{th} **variation is instead perfectly correlated** within a die, which group is expected to have worse 99th percentile delay, or are 99th percentile delays equal? **Explain.**

The delays are equal. Since we have perfect correlation, Cone 2 will be affected exactly the same as Cone 1.

c) **(5 Points)** Consider the following four scenarios where each considers one output/logic cone and either correlated or uncorrelated variation. Please order the scenarios from largest to smallest sigma of output transition time in *absolute* terms.

Scenario 1: Output O1, logic cone 1: V_{th} variation is uncorrelated

Scenario 2: Output O2, logic cone 2: V_{th} variation is uncorrelated

Scenario 3: Output O1, logic cone 1: V_{th} variation is perfectly correlated

Scenario 4: Output O2, logic cone 2: V_{th} variation is perfectly correlated

Scenario Number

Largest sigma ________
___3=4___
___2___
Smallest sigma ___1___

4.0 Problem 4 (12 Points) – SRAM

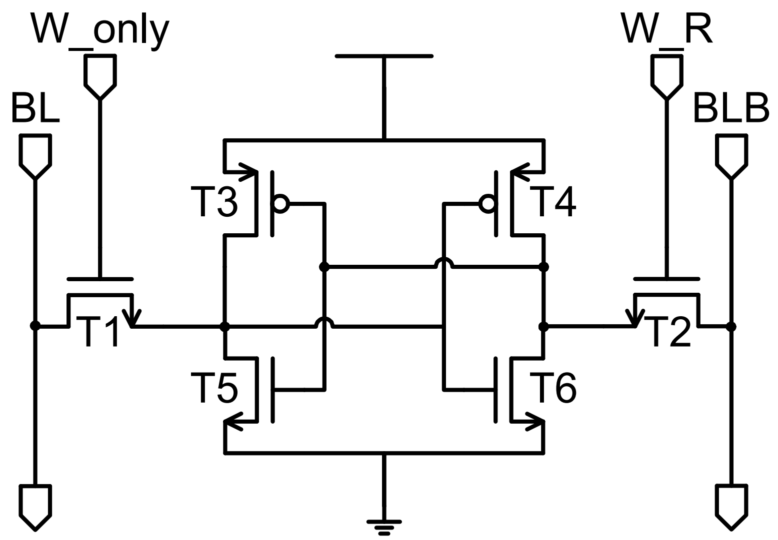


Figure 4. SRAM Circuit for Problem 4.0.

The circuit above is similar to a traditional 6T-SRAM with **one major difference**:on a write, **both** *W_only* and *W_R* go high (writing the SRAM from both sides); on a read, **only** *W_R* goes high, reading the value onto *BLB*.

4.1 (4 Points) How would you modify transistors T1 – T6 to test for **write robustness**? **Assume only V_{th} variation matters**. For each transistor in Figure 5 below, circle the correct value to skew V_{th} by, either -3σ or +3σ to test for worst case robustness.

NOTE: Notice the existing node voltages within the SRAM, as well as the values we're trying to write.

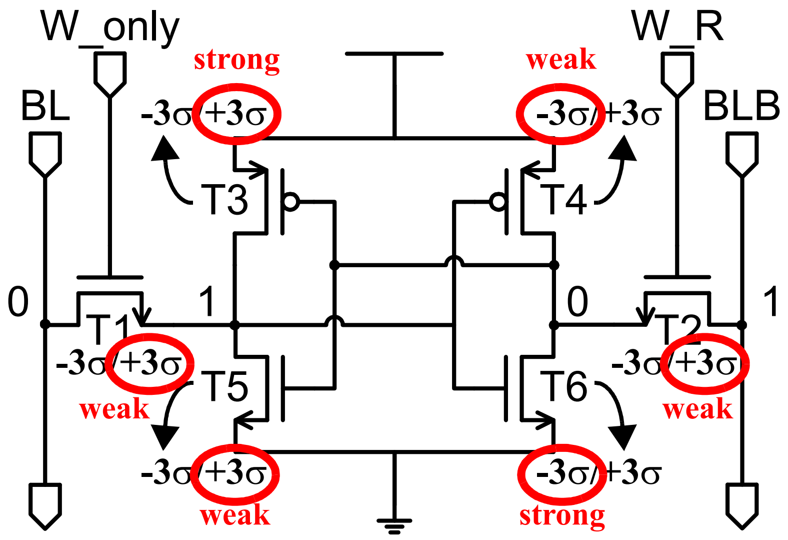


Figure 5. SRAM Circuit for Problem 4.1.

4.2 (4 Points) How would you modify transistors T1 – T6 to test for **read robustness**? Similar to Problem 4.1, for each transistor in Figure 6 below, circle the correct value to skew V_{th} by, either -3σ or +3σ to test for worst case robustness.

NOTE: The internal node voltages of the SRAM cell are the same as Problem 4.1.

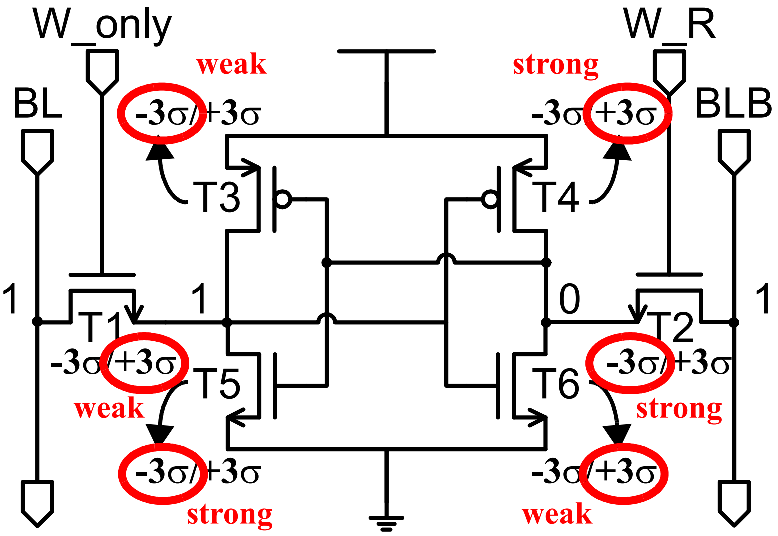


Figure 6. SRAM Circuit for Problem 4.2.

4.3 (4 Points) While sizing the SRAM cell from Figure 4 for robustness, what will the relative transistor sizings be for transistor pairs [T1,T2] and [T5,T6]. **Fill in the blanks below (fill in "greater than," "less than," or "equal" between pairs). Explain.**

(e.g., T3 greater than T4)

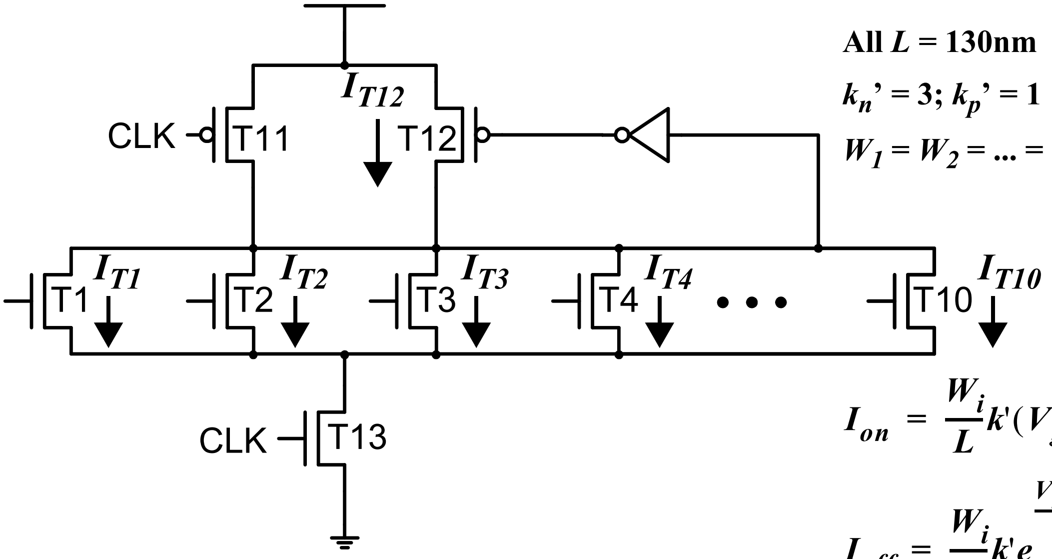
T1 ___greater than___ T2

T5 _____less than_____ T6

Explain: **We want transistor T1 sized up for write robustness (for both writing a "0" on BL as well as a "1") but T2 shouldn't be sized up as much due to the fact that it hurts read robustness. Therfore, T1's size should be "greater than" T2's.**

Also, we would like T6 sized up for read robustness and T5 somewhat sized down for read robustness (read "1" robustness) and write robustness (write "0" robustness). Therefore, T5's size will be "less than" T6's.

5.0 Problem 5 (19 Points) – Dynamic Logic Sizing & Robustness



All L = 130nm

k_n’ = 3; k_p’ = 1

$W_1 = W_2 = ... = W_{10}$ = 400nm

$$I_{on} = \frac{W_i}{L}k'(V_{gs} - V_{th})^{1.5}$$

$$I_{off} = \frac{W_i}{L}k'e^{\frac{V_{gs} - V_{th}}{nV_T}}$$

Figure 7. 10-input dynamic NOR gate with keeper for Problem 5.0.

Circuit Parameters: V_{DD} = 1.2V; $V_{th,n}$ = 0.4V; $V_{th,p}$ = -0.4V; n = 3.5; V_T = 26mV.

Consider the 10-input dynamic NOR gate shown in the figure above and use the information provided to answer the following questions.

5.1 (8 Points) Provide an *inequality* that constrains the sizing of W_{12} (the keeper’s gate width) during the *evaluation* phase of the clock, given that $W_1 = W_2 = ... = W_{10}$ **= 400nm**.

- **Ignore the drive current through T_{13}.**
- **Ignore the leakage current through T_{11}.**

$$I_{on,\,T12} > \sum_{i=1}^{10} I_{off,\,i}$$

$I_{on,\,T12} < I_{on,\,j} \quad \forall j \in [1, 10]$ **(Ignoring I_{off} for other 9 transistors)**

$$10 \cdot \frac{400\text{nm}}{130\text{nm}} \cdot 3 \cdot e^{\frac{-0.4}{3.5 \cdot 0.026}} < \frac{W_{12}}{130\text{nm}} \cdot 1 \cdot (|-1.2-(-0.4)|)^{1.5} < \frac{400\text{nm}}{130\text{nm}} \cdot 3 \cdot (1.2-0.4)^{1.5}$$

$$12000\text{nm} \cdot 0.01233 < W_{12} \cdot 0.7155 < 1200\text{nm} \cdot 0.7155$$

$$\Rightarrow 206.804\text{nm} < W_{12} < 1200\text{nm}$$

5.2 (11 Points) After performing the initial sizing analysis from Problem 5.1, the process engineers inform you of the die-to-die and within-die distributions of V_{th} variation (*the nominal* V_{th} *is still* $+0.4V$ and $-0.4V$ for NMOS and PMOS devices, respectively). They are as follows:

$[\mu_{die\text{-}to\text{-}die}, \sigma_{die\text{-}to\text{-}die}] = [0, 40\text{mV}]$

$[\mu_{within\text{-}die}, \sigma_{within\text{-}die}] = [0, 30\text{mV}]$

NOTE: The within-die variation is perfectly *independent and uncorrelated.*

Assuming that V_{th} is the only type of variation, *will your sizes from Problem 5.1* still work with worst case ($\pm 3\sigma$) variation considering:

(1) die-to-die variation (D2D), only

(2) both die-to-die variation (D2D) and within-die variation (WD)?

(5 Points) **Scenario 1 (D2D, only): Circuit will (work/not work)** work

Explain:

D2D variation affects all transistors the same (Note: higher $V_{th,p}$ is more negative) →

$$V_{th,p} = -0.4 - \text{D2D}$$
$$V_{th,n} = 0.4 + \text{D2D}$$

$$12000\text{nm} \cdot e^{\frac{-(0.4+\text{D2D})}{3.5 \cdot 0.026}} < W_{12} \cdot (|-1.2 + 0.4 + \text{D2D}|)^{1.5} < 1200\text{nm} \cdot (1.2 - 0.4 - \text{D2D})^{1.5}$$

$$\Rightarrow \frac{12000\text{nm} \cdot e^{\frac{-(0.4+\text{D2D})}{3.5 \cdot 0.026}}}{(|-1.2 + 0.4 + \text{D2D}|)^{1.5}} < W_{12} < 1200\text{nm}$$

Case 1: D2D = +120mV

$$\frac{12000\text{nm} \cdot e^{\frac{-(0.4+0.12)}{3.5 \cdot 0.026}}}{(|-1.2 + 0.4 + \text{D2D}|)^{1.5}} < W_{12} < 1200\text{nm}$$

$$\Rightarrow 70.589\text{nm} < W_{12} < 1200\text{nm}$$

Case 2: D2D = –120mV

$$\frac{12000\text{nm} \cdot e^{\frac{-(0.4-0.12)}{3.5 \cdot 0.026}}}{(|-1.2 + 0.4 + \text{D2D}|)^{1.5}} < W_{12} < 1200\text{nm}$$

$$\Rightarrow 626.915\text{nm} < W_{12} < 1200\text{nm}$$

So as long as you picked a size for the keeper that is greater than 626.915nm but less than 1200nm, then the circuit will still work.

(Note that the worst case constraint happens due to higher leakage where D2D = –120mV.)

(6 Points) Scenario 2 (D2D + WD): Circuit will (work/not work) not work

Explain:

$$12000 \cdot e^{\frac{-(0.4 + \mathrm{D2D} + \mathrm{WDi})}{3.5 \cdot 0.026}} < W_{12} \cdot (|-0.8 + \mathrm{D2D} + \mathrm{WD12}|)^{1.5} < 1200 \cdot (0.8 - \mathrm{D2D} - \mathrm{WDj})^{1.5}$$

$$\Rightarrow \frac{12000\mathrm{nm} \cdot e^{\frac{-(0.4 + \mathrm{D2D} + \mathrm{WDi})}{3.5 \cdot 0.026}}}{(|-0.8 + \mathrm{D2D} + \mathrm{WD12}|)^{1.5}} < W_{12} < \frac{1200\mathrm{nm} \cdot (0.8 - \mathrm{D2D} - \mathrm{WDj})^{1.5}}{(|-0.8 + \mathrm{D2D} + \mathrm{WD12}|)^{1.5}}$$

Case	D2D (mV)	WDi (mV)	WD12 (mV)	WDj (mV)	
1	+120	+90	+90	+90	$\frac{12000\mathrm{nm} \cdot e^{\frac{-(0.4+0.12+0.09)}{3.5 \cdot 0.026}}}{(\lvert -0.8+0.12+0.09 \rvert)^{1.5}} < W_{12} < \frac{1200\mathrm{nm} \cdot (0.8-(0.12+0.09))^{1.5}}{(\lvert -0.8+0.12+0.09 \rvert)^{1.5}}$ $\Rightarrow 32.486\mathrm{nm} < W_{12} < 1200\mathrm{nm}$
2	+120	+90	+90	–90	$\frac{12000\mathrm{nm} \cdot e^{\frac{-(0.4+0.12+0.09)}{3.5 \cdot 0.026}}}{(\lvert -0.8+0.12+0.09 \rvert)^{1.5}} < W_{12} < \frac{1200\mathrm{nm} \cdot (0.8-(0.12-0.09))^{1.5}}{(\lvert -0.8+0.12+0.09 \rvert)^{1.5}}$ $\Rightarrow 32.486\mathrm{nm} < W_{12} < 1789.119\mathrm{nm}$
3	+120	+90	–90	–90	$\Rightarrow 21.789\mathrm{nm} < W_{12} < 1200\mathrm{nm}$
4	+120	+90	–90	+90	$\Rightarrow 21.789\mathrm{nm} < W_{12} < 804.865\mathrm{nm}$
5	+120	–90	–90	+90	$\Rightarrow 157.501\mathrm{nm} < W_{12} < 804.865\mathrm{nm}$
6	+120	–90	–90	–90	$\Rightarrow 157.501\mathrm{nm} < W_{12} < 1200\mathrm{nm}$
7	+120	–90	+90	–90	$\Rightarrow 234.824\mathrm{nm} < W_{12} < 1789.119\mathrm{nm}$
8	+120	–90	+90	+90	$\Rightarrow 234.824\mathrm{nm} < W_{12} < 1200\mathrm{nm}$
(For brevity, skip to interesting cases when D2D = –120mV)					
15	–120	–90	+90	–90	$\Rightarrow 1966.960\mathrm{nm} < W_{12} < 1610.817\mathrm{nm}$
16	–120	–90	+90	+90	$\Rightarrow 1966.960\mathrm{nm} < W_{12} < 1200\mathrm{nm}$

In Cases 15 & 16 (among others), you find that you have unsatisfiable inequalities. Therefore, no matter what sizing you pick for the keeper, the circuit will not work with this much variation.

6.0 Problem 6 (6 Points) – Problems in High-Power Design

List three of the major problems that are introduced by having a very high-power chip design.

1)Heat becomes a large issue; affects packaging

2)Electromigration worsens

3)Large currents drains lead to larger IR drops

4)L dI/dt will change your supply voltages

5) (3) and (4) cause noise margins to worsen

7.0 Problem 7 (6 Points) – Verilog

Consider the following verilog module:

```
module test_question;
reg [3:0] c, d, e, f;

initial begin
   c = 3;
   #1 c = c + 1;
   d = c + 1;
   #1  //t = 2, question part (a)
   #1 e = 3;
   #1 e <= e + 1;
   f <= e + 1;
   #1  //t = 5, question part (b)
   end
endmodule
```

a) At time t = 2, what are the values of registers ‘c’ and ‘d’?

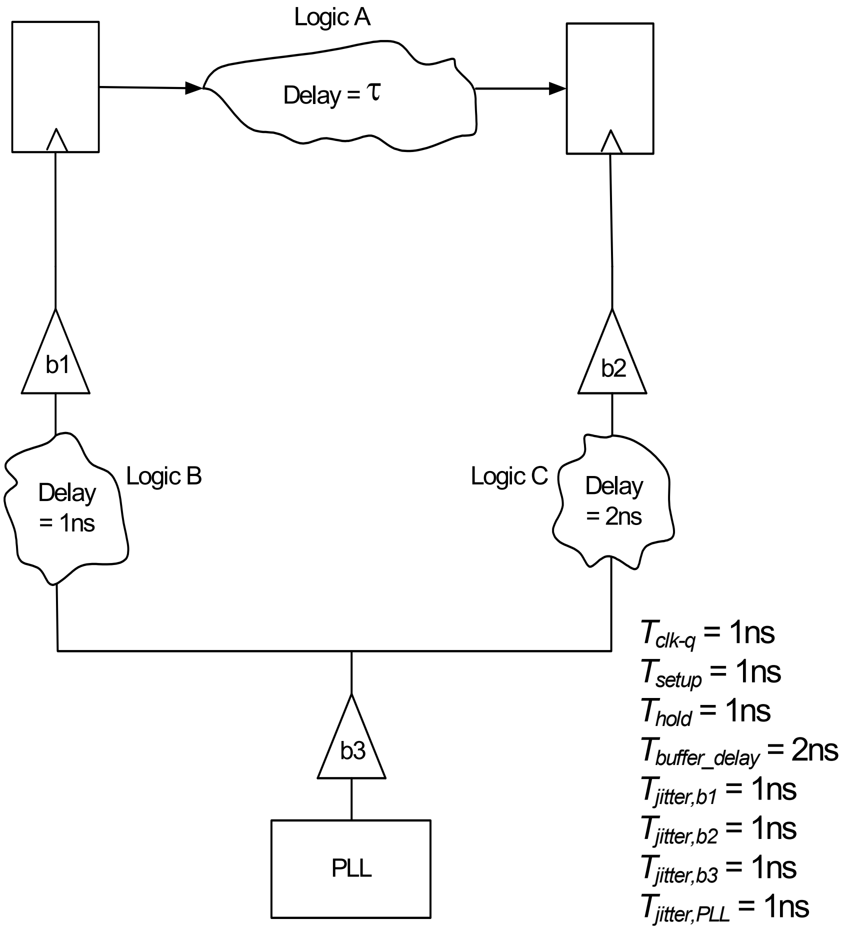
Here we have blocking assignments, so first c becomes ‘4’, then d is assigned ‘5’.

b) At time t = 5, what are the values of registers ‘e’ and ‘f’?

Now we have non-blocking assignments. Both ‘e’ and ‘f’ are assigned simultaneously using the initial value of ‘e’, so e = f = 4.

8.0 Problem 8 (17 Points) – Timing & Synchronization

The following circuit is operated with a clock period of 10ns.



$T_{clk\text{-}q}$ = 1ns
T_{setup} = 1ns
T_{hold} = 1ns
T_{buffer_delay} = 2ns
$T_{jitter,b1}$ = 1ns
$T_{jitter,b2}$ = 1ns
$T_{jitter,b3}$ = 1ns
$T_{jitter,PLL}$ = 1ns

Figure 8. Circuit for Problem 8.0.

a) **(4 Points)** Which of the circuit elements shown in the diagram could introduce *skew* and why?

b1, b2, Logic B and Logic C introduce skew. b3 and PLL do not because the are on the common part of the clock path.

b) **(6 Points)** Assume all delays are at their nominal values as shown. **Excluding jitter**, what is the *minimum* and *maximum* delay of **Logic A (i.e., what is** τ)? **Give both numerical solutions and equations, indicating clearly the source of each delay.** *Your answers should be in the form "x < τ < y ".*

Max $\tau = T_{clk} - T_{setup} - T_{clk\text{-}q} + \text{skew} = 10 - 1 - 1 + 1 = 9\text{ns}$ (skew is positive in this example)

Min $\tau = T_{hold} - T_{clk\text{-}q} + \text{skew} = 1 - 1 + 1 = 1\text{ns}$

$1\text{ns} < \tau < 9\text{ns}$

$T_{hold} - T_{clk\text{-}q} + \text{skew} < \tau < T_{clk} - T_{setup} - T_{clk\text{-}q} + \text{skew}$

c) **(7 Points)** Repeat part (b), but now **include the effects of jitter**. Assume that the three buffers and the PLL can each introduce a maximum *cycle-to-cycle* jitter of 1ns, and that these values are uncorrelated. Clearly show and explain your equations. Again, clearly indicate the source of each delay. (For example, instead of generically writing T_{jitter}, write $T_{jitter}(b_x)$ to indicate a particular jitter term comes from buffer b_x).

Max $\tau = T_{clk} - T_{setup} - T_{clk\text{-}q} + skew - T_{jitter,PLL} - T_{jitter,b1} - T_{jitter,b2} - T_{jitter,b3}$

Min $\tau = T_{hold} - T_{clk\text{-}q} + skew + T_{jitter,b1} + T_{jitter,b2}$

3ns < τ < 5ns

$$\mathbf{T_{hold} - T_{clk\text{-}q} + skew + T_{jitter,b1} + T_{jitter,b2} < \tau < T_{clk} - T_{setup} - T_{clk\text{-}q} + skew - T_{jitter,PLL} - T_{jitter,b1} - T_{jitter,b2} - T_{jitter,b3}}$$