EECS 427: VLSI Design I
Fall 2009 Syllabus, Revised 9/7/09

Texts: Default = Rabaey, WH = Weste and Harris, CBF = Chandrakasan, Bowhill, and Fox

Date	**Topic**	**Reading/Coverage**	**Notes, assignments due**
September 9	Course Introduction, Manufacturing	1.1-1.3 (review), 2.2, WH 3.2	Tutorial1 (7-9pm)
9/14	Design Rules & Layout	2.3, Insert A, WH 1.5, WH 3.3	
9/16	CMOS Review	5.4, 6.2	CAD1 due
9/21	Logical Effort	handouts	HW1 due CAD2 due
9/23	Logical Effort	handouts	
9/28	Logic Styles	6.2	HW2 due (teams)
9/30	Adders	11.1-11.3.1	CAD3 due
October 5	Adders	11.3.2-11.3.3	
10/7	Shifters	11.5, WH 10.8	HW3 due (initial proposal)
10/12	Multipliers	11.4	
10/14	Quiz 1		CAD4 due
10/19, 10/20 - Fall Study Break, No Classes			
10/21	Power and Energy	5.5	
10/26	Dynamic Power Reduction	11.7, CBF Ch. 4	
10/28	Leakage Power Reduction	6.4.2, CBF Ch. 3	CAD5 due
November 2	Dynamic Logic	6.3	
11/4	Interconnects	4.3.1, 4.3.2, 4.4.1-4.4.3, 9.3.3	CAD6 due
11/9	Design Styles, Synthesis	8.1-8.4	
11/11	Timing, skew/jitter	10.1-10.3	CAD7 due
11/16	Timing cont., D-Q, pulsed latches	10.3, 7.4	HW4 due (detailed proposal)
11/18	Memory Core and Peripherals	12.1-12.3	CAD8 due
11/23	Quiz 2		
11/25	Memory Reliability and Power	12.4, 12.5	
11/26, 11/27 - Thanksgiving Break, No Classes			
11/30	Design-for-Test (DFT)	Insert H.3, CBF Ch. 25	
December 2	Clock Distribution & Robustness	10.3.3, 10.6, CBF Ch. 13	
12/7	Advanced Interconnect Techniques	9.5	
12/9	Power Grid and Other Issues	WH 12.3, CBF Ch. 24	Course evaluations in class
12/14	Final Project Demos Final Project Presentations		CAD9: final due HW5 due (report) HW6 (presentation)

Summary of *tentative* due dates:

All HWs due at 1:30pm before class.
HW1 (problem set): Monday, Sept. 21
HW2 (teams): Monday, Sept. 28
HW3 (initial proposal): Wednesday, Oct. 7
HW4 (detailed proposal): Monday, Nov. 16
HW5 (final report): Monday, Dec. 14
HW6 (project presentations): Monday, Dec. 14

All CADs due at 7pm except CAD9.
CAD1 (inverter/nand/mux): Wednesday, Sept. 16 (1 week)
CAD2 (D flip-flop): Monday, Sept. 21 (5 days)
CAD3 (register file): Wednesday, Sept. 30 (1+ week)
CAD4 (ALU): Wednesday, Oct. 14 (2 weeks)
CAD5 (shifter): Wednesday, Oct. 28 (2 weeks)
CAD6 (program counter): Wednesday, Nov. 4 (1 week)
CAD7 (datapath): Wednesday, Nov. 11 (1 week)
CAD8 (controller): Wednesday, Nov. 18 (1 week)
CAD9 (project completion/demo): Monday, Dec. 14 (~4 weeks)