CAD1   Inverter/Nand/2:1 Mux   Fall 2010

Assignment

Create schematics, symbols, and layouts for an inverter and a 2-input nand gate. Using these symbols and layouts, create a schematic, symbol, and layout for a 2:1 mux using 3 2-input nand gates and 1 inverter. Perform design-rule-checks (DRC) and a layout-vs.-schematic (LVS) check on the layouts of the inverter, 2-input nand, and 2:1 mux. Then, get accurate propagation delays for the 2:1 mux by extracting parasitic capacitances from the layout and simulating the circuit with *HSpice*.

You probably will not use any of these cells in your final project, so don't be concerned about choosing the optimal transistor sizes. Try to **minimize area** and feel free to use Metal 1, Metal 2, and Metal 3 for routing. The first two cad assignments are to be done on your own. You may discuss use of the cad tools and basic layout concepts with other students, but your design, particularly your layout, should be created by yourself.

Description

- Create a directory in your class account called **cad1**. All of your files will need to be in this directory in order to be graded.
- Make the **schematics** and **symbols** for the inverter and 2-input nand using *Composer*. Name you 2-input nand, "nand2," and your 2:1 mux, "mux2." Be sure to use the pfet/nfet transistors from the library "cmrf8sf". Call the inverter ports **in** and **out**. Call the nand ports **in0**, **in1**, and **out**. Call the mux2 ports **in0**, **in1**, **sel**, and **out**.
- **Simulate** the inverter and nand in *NC Verilog* and verify correct functionality. Test all possible inputs for both gates. Create the input stimulus as you did in the inverter tutorial by editing the testfixture.verilog file to forces the inputs.
- Follow the guidelines of *The Design and Simulation of an Inverter* to create layouts for the inverter and 2-input nand. Make sure that you use the same names to label the inputs and outputs of the gates in *Virtuoso Layout Editor (VLE)* that are used on the symbol. Keep in mind when designing these gates that they will be used in the layout of the 2:1 mux. Examples of things to keep in mind:
  - (1) How will you route between the 4 cells?
  - (2) How will you place the cells to create a 2:1 mux?
  - (3) Where will you place your input and output ports?

  For example, you could place all your cells in a straight line or in a square. **Choose a configuration that minimizes interconnect length.**
- Perform a Design Rules Check (**DRC**) on the layouts of the inverter and nand gates. For directions please refer to *The Design and Simulation of an Inverter*. DRC report should be saved automatically under **Calibre/DRC/<component_name>.drc.summary**. If not, please save it.
- Perform a Layout Versus Schematic (**LVS**) on the layouts of the inverter and nand gates. For directions please refer to *The Design and Simulation of an Inverter*. LVS report should be saved automatically under **Calibre/LVS/<component_name>.lvs.report**. If not, please save it.
- Make the **schematics** and **symbols** for the 2:1 mux and call it **mux2**. Create the 2:1 mux by instantiating 3 of your nand gates and 1 inverter.
- **Simulate** the 2:1 mux in *NC Verilog* and verify correct functionality. Force values on the two inputs and select such that all possible input combinations are accounted for.
- Follow the guidelines of *The Design and Simulation of an Inverter* to create layout for the 2:1 mux. **The only structures that you may use in the 2:1 mux are the cells created earlier in this CAD assignment and metal1, metal2, metal3, or polysilicon to connect those cells.** Make sure that you use the same names to label the inputs and outputs of the 2:1 mux in VLE that are used on the symbol. Also try to minimize your use of upper metal layers.

- Perform a Design Rules Check (**DRC**) on the layouts of the 2:1 mux. Check if DRC reports are saved.
- Perform a Layout Versus Schematic (**LVS**) on the layout of the 2:1 mux. Check if LVS report is saved.
- Extract the capacitance values from the 2:1 mux. For directions, please refer to *The Design and Simulation of an Inverter*.
- Use *HSpiceD* to simulate the circuit in the spice domain. Refer to the inverter tutorial for details as to how to use it. Prior to doing this, set the output capacitance to 25fF to represent the load on the mux. Find the propagation delay of the mux2 cell.

Requirements

For the first CAD experiment, you need to have the following files:
- inverter, 2-input nand and 2:1 mux schematics and layouts.
- Waveform files for all *NC Verilog* simulations. (All three circuits)
- Wave .png of the critical path waveforms generated by *HSpice*.
- DRC, and LVS report for the inverter, 2-input nand, and 2:1 mux.
- The height and width for inverter, nand and mux should be a multiple of 0.4um
- Use hierarchical method to create the schematic and the layout for your 2:1 mux
- Include a README file containing the full path names for all of the cells the grader is to look at, and any comments you wish to pass on to the grader. Include in the file the maximum rise and fall times. List the nodes between which the rise and fall delays were maximum, what that delay was, and explain why that path was the maximum. Provide a brief paragraph describing any relevant points in your design. Any comments will be taken into consideration when your assignments are graded.
- You need to name your directory **cad1**, and create a "**submit**" directory in your **cad1** directory. Copy all your drc, lvs reports, and simulation waveform files to the "**submit**" directory.

For this and future cad assignments, follow these submission guidelines:
- Please name your README file README (not readme, readthis, info, cad1_readme, etc.); README should be in your cad directory instead of submit directory
- Naming convention for the drc_reports: <component_name>.drc.summary
- Naming convention for the lvs reports: <component_name>.lvs.report
- Naming convention for the spice waveforms: spice_<component_name>_<description>.png Where <description> is a brief description of the measurement (e.g. falltime, risetime, falldelay, risedelay)
- Naming convention for the *NC Verilog* waveforms: nc_<component_name>.ps. Make sure this waveform shows proper digital functionality of your design and explain in the readme why this input set was sufficient i.e. covered all possible input combinations exhaustively.

Deadline

You have to complete the first CAD assignment by **Thursday, Sept. 16, 2010, 11pm.**