

## Assignment

To design a register cell and find timing characteristics.

## Description

In this CAD assignment, you will design, layout and simulate a 1-bit register (flip-flop) cell. Your full-custom datapath will require a couple of multi-bit registers and you should design this 1-bit register as a bit-sliced component for this purpose. You probably won't use this cell in your final datapath, but this exercise will introduce you to complex leaf-cell design as well as datapath style layout concepts. Note that once again you must work on your own for this assignment.

## Implementation

It is often desirable to be able to reset asynchronously the state of the register to a known value (usually zero). A typical gate implementation of a positive edge-triggered master-slave D flip-flop is shown in Figure 1.

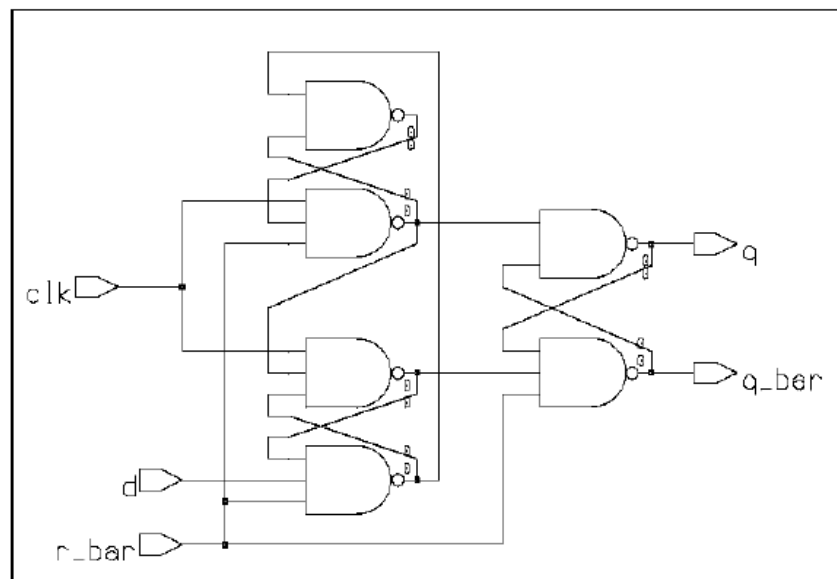


Figure 1: Positive Edge Triggered Flip-Flop Using Logic Gates

An example for a static CMOS transmission gate-based implementation is shown in Figure 2. Use of this design, or similar designs more adapted to CMOS technology, would result in many fewer transistors than the flip-flop of Figure 1, and it is not recommended that Figure 1 be used. Note that a conceptually simpler starting point would be a flip-flop composed of two latches (connected in master/slave configuration) like the master latch in Figure 2 (which is still not being held up as the best design).

The flip-flop could be further compacted by using a dynamic or pseudo-dynamic style with two-phase or single-phase clocking, but we do not support dynamic design styles for EECS 427.



## Analog Simulation

Extract the parasitic capacitances and run spice on the D flip-flop and obtain the rise and fall CLK-Q delay times as well as the rise and fall setup and hold times for the D flip-flop. (Exactness is not required for the calculation of setup time, but you should try to get a relatively accurate estimate). Remember to add the 25fF capacitor to the output node to account for the load that the flip-flop may drive. Use the cursors to find your delay estimates. Save an image of your waveforms with the cursors in place that helped you calculate the delay.

## Setup time/Hold time measurement

### Setup

- Store a 1 (0) to the flip-flop and allow to settle for one clock cycle
- Next clock cycle, change D input  $\geq 0.25$  clock cycle **before** rising edge and measure CLK-Q delay (50% CLK  $\rightarrow$  50% Q)
- Run parametric sweep adjusting D transition later and later – closer to rising edge of CLK (make sure hold time is long too,  $\geq 0.25$  clock cycle, otherwise hold will affect too!!)
- Setup constraint is time in parametric sweep which causes  $\approx 5\%$  increase in CLK-Q delay (calculated in 2<sup>nd</sup> step)

### Hold

- Store a 1 (0) to the flip-flop and allow to settle for one clock cycle
- Next clock cycle, change D input  $\geq 0.25$  clock cycle **after** rising edge and measure CLK-Q (should be similar to 2<sup>nd</sup> step of setup time)
- Run parametric sweep make D transition earlier and earlier (making sure setup time is long,  $\geq 0.25$  clock cycle)
- Hold constraint is time in parametric sweep which causes  $\approx 5\%$  increase in CLK-Q delay (calculated in 2<sup>nd</sup> step)

## Requirements

You should have the following files:

- Schematic of your D flip-flop.
- Layout of the D flip-flop
  - Height/width should be a multiple of 0.4 $\mu$ m,
  - M2, M3 should be on grid.
- NC Verilog waveform files showing functional verification of your 1-bit register.
- NC Verilog waveform files with delay added.
- Spice waveforms (after pex) for the following:
  - Rise and fall CLK-Q delays
  - Setup and hold times for each (rise and fall).Rise/fall delays are measured from the 50% point of CLK to 50% of the Q output transition. You do not have to be exact about the setup time – just get within a few picoseconds.
- DRC and LVS reports
- Briefly describe each simulation in your README file.
- A README file with the names and paths of all of the requested files. Include a few paragraphs describing your design and verification rationale.
- You need to name your directory **cad2**, and create a “**submit**” directory in your **cad2** directory. Copy all your drc, lvs reports, and simulation waveform files to the “**submit**” directory.

## Deadline

You need to turn CAD2 in by Thursday, **Sep. 23, 2010, 11pm.**