EECS 427 W09
Discussion 1

Wei-Hsiang Ma

2009/01/16

Announcement

- Out of town next week
- Jerry(previous 427/627 GSI) will cover my office hr and the discussion. (jckao@umich.edu)
- Office hour: Tues/Thurs 3:30~8:30 (only next week), same place
- You can still reach me by e-mail

Today

- Some important things you need to know for the layout
- Tutorial 1.5 and CAD2
- Tutorial 1 questions, CAD1 questions, other questions

Metal layer usage

- Which one is better if you want to do a connection between cells

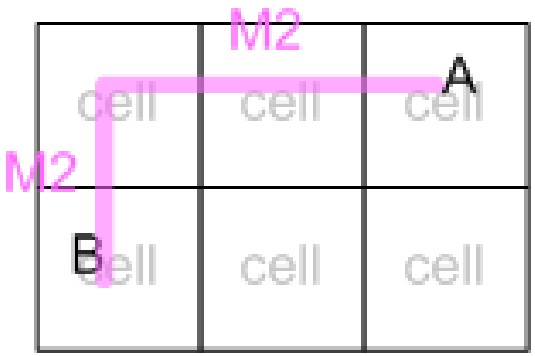


Fig 1

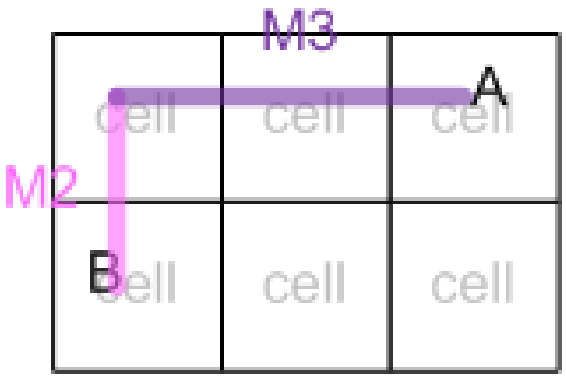


Fig 2

Fig 1 is easier but Fig2 can give you more M2/M3 tracks within the same area

Metal layer usage (continue)

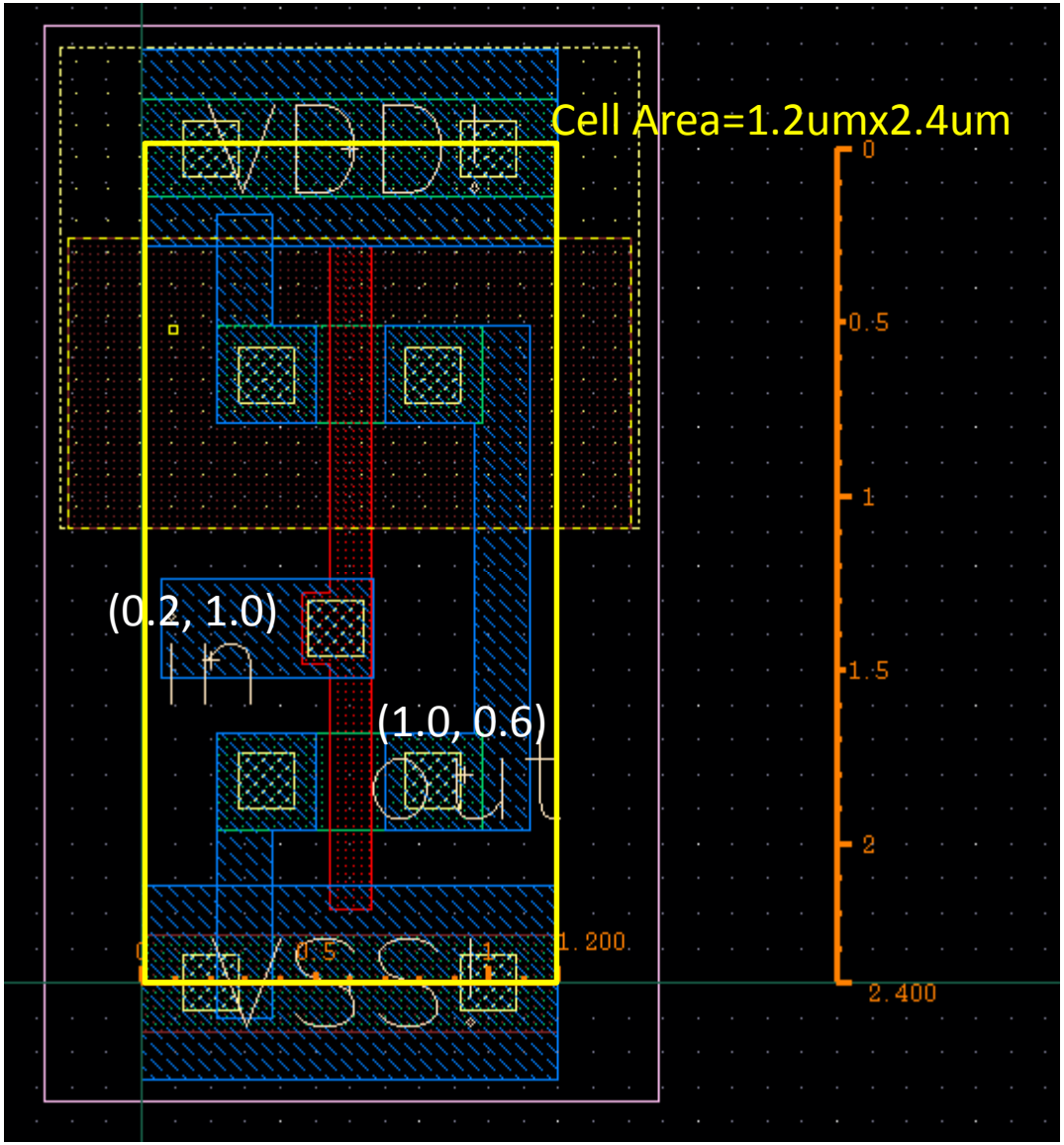
- Connection
  - Inside the cell:
    - PC and M1, M1 is preferred, since R is smaller
  - Connections between cells and cells
    - Vertical connection M2, M4, M6
    - Horizontal connection M3, M5
  - Imagine there are virtual routing tracks
    - In design rules, Metal and Metal space is 0.2um, Metal minimum width is 0.2um.
    - 0.4um per track

Metal layer usage (continue)

- We ask you follow our track requirement. All M2, M3, M4, M5, M6 routing should be on the track.

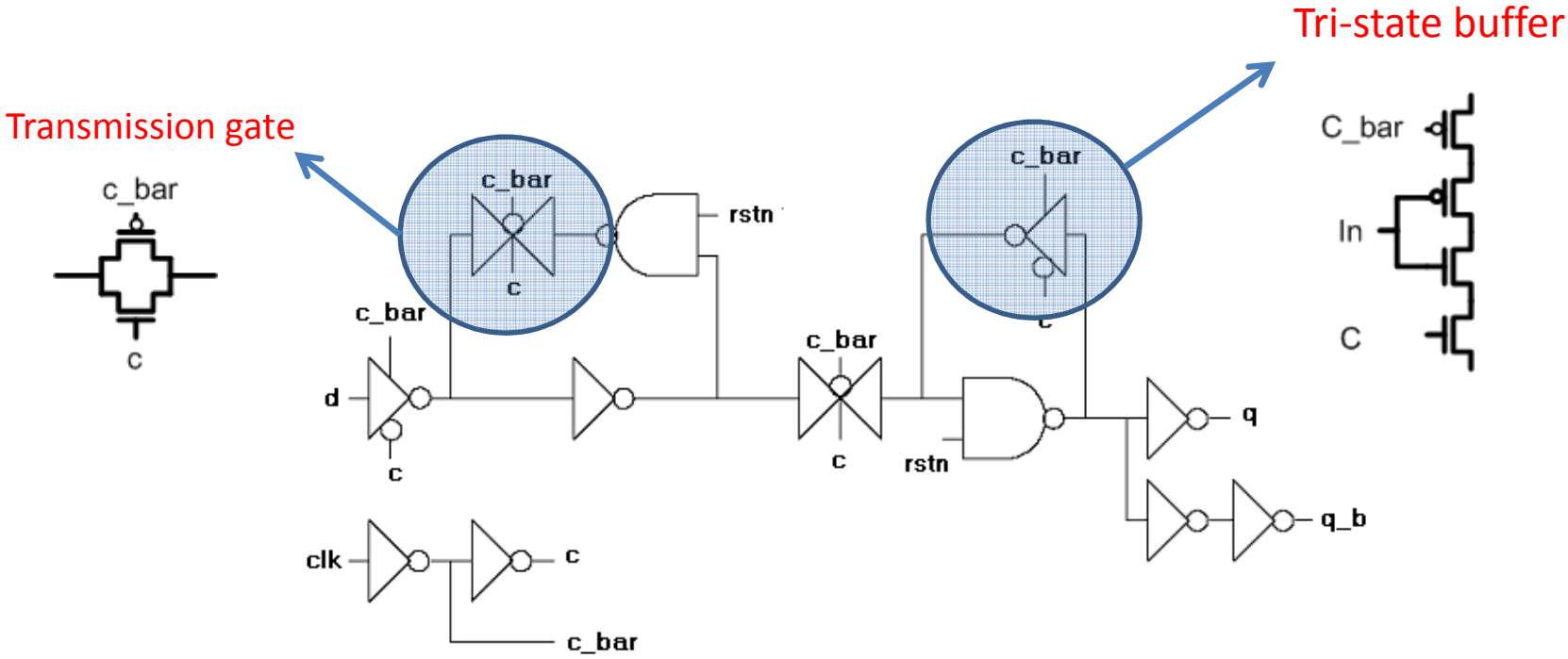
  Three principles:

  – Set the origin, and then put labels on the grid.
  – Make the cell height/width as multiple of 0.4um
  – Do the routing on track.
  – Follow the above two principles will make your CAD easier.


Cell Area=1.2umx2.4um
(0.2, 1.0)
(1.0, 0.6)
VDD
VSS
OUT
0
0.5
1
1.5
2
2.400
1.200

1-bit register (flip-flop)

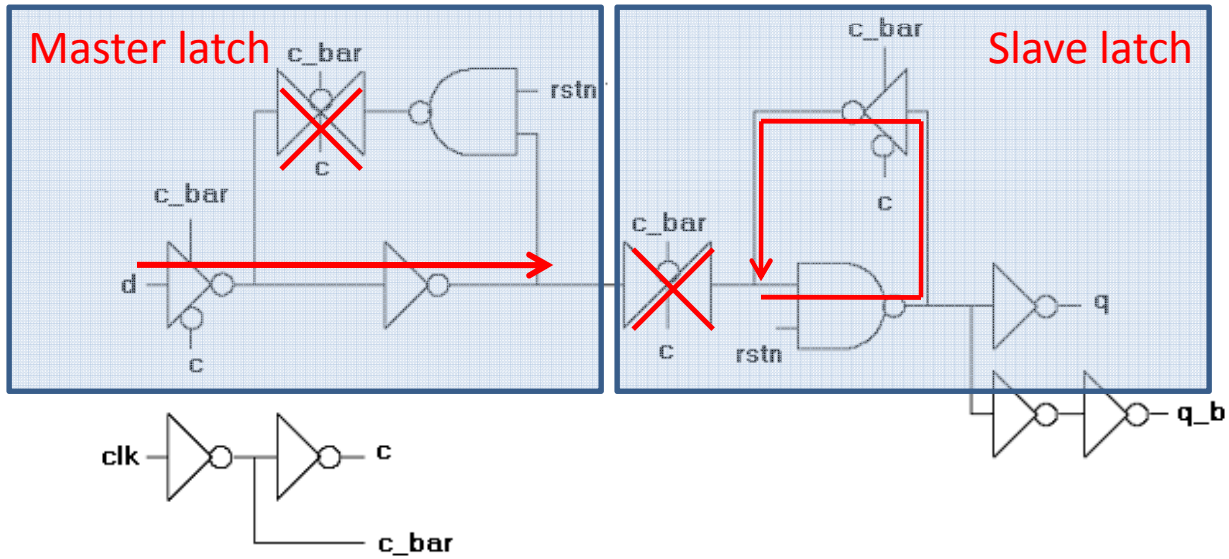
- Schematic
  - Clk= clock, d = input, rstn = reset
  - Asynchronous reset: as reset goes low, q is set to 0 (this example)
  - Synchronous reset: when clk goes high, it will check if reset is low, if it is, then set q to 0.
  - Asynchronous v.s. Synchronous = reset triggered v.s. clk triggered



Register (continue)

- How it works

  When C is equal to 0, the master latch is transparent, and the salve latch is closed.

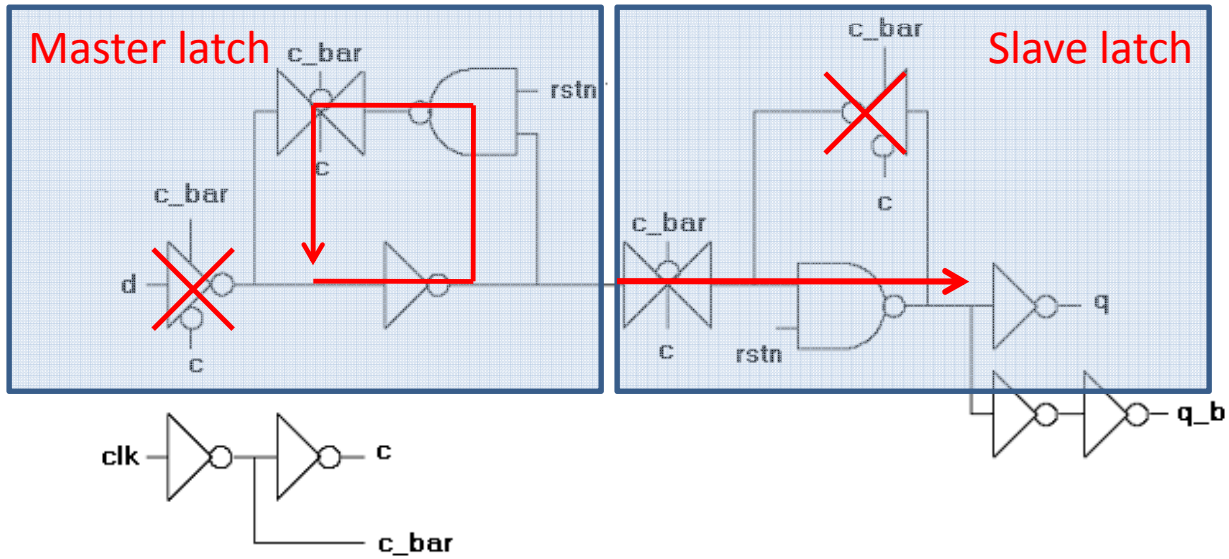


Register (continue)

- How it works

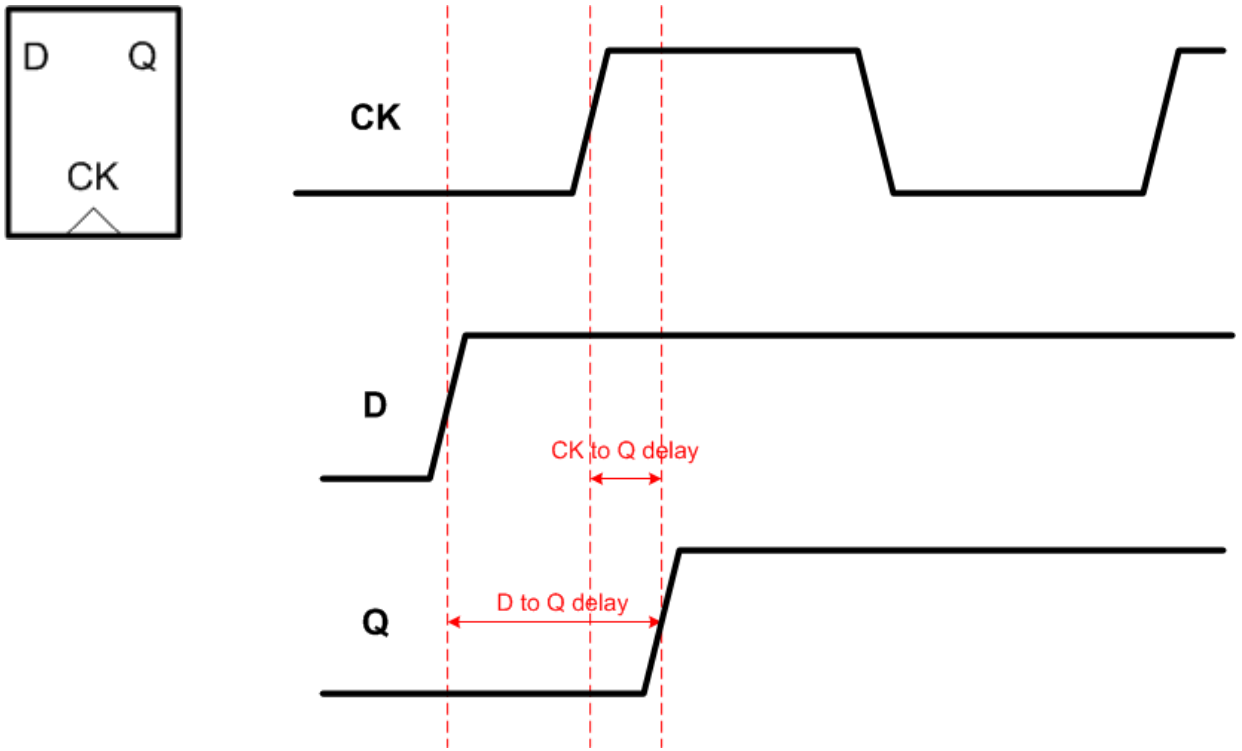
  When C is equal to 1, the master latch is closed, and the salve latch is transparent

  When C switches from 0->1 (rising edge of the clock) the register captures the data .



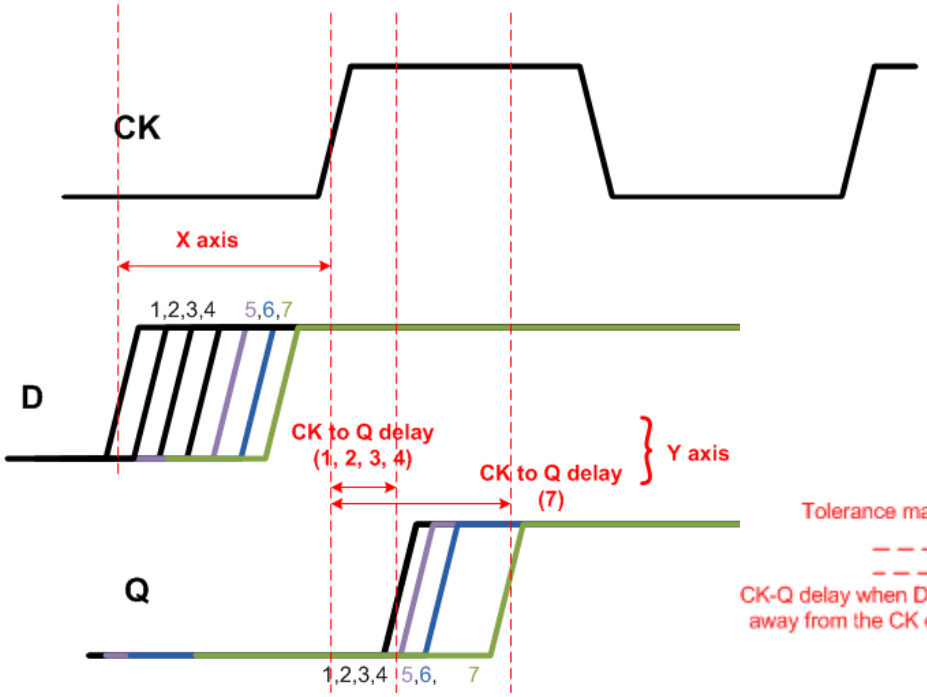
Register (continue)

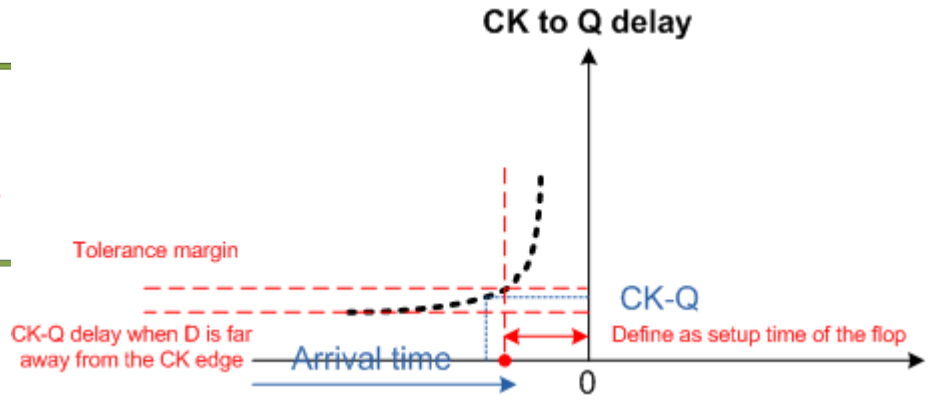
- Important terms,(C-Q delay, D-Q delay)



Register (continue)

- Setup Time
- As D approaches to CK edge, C-Q delay goes up

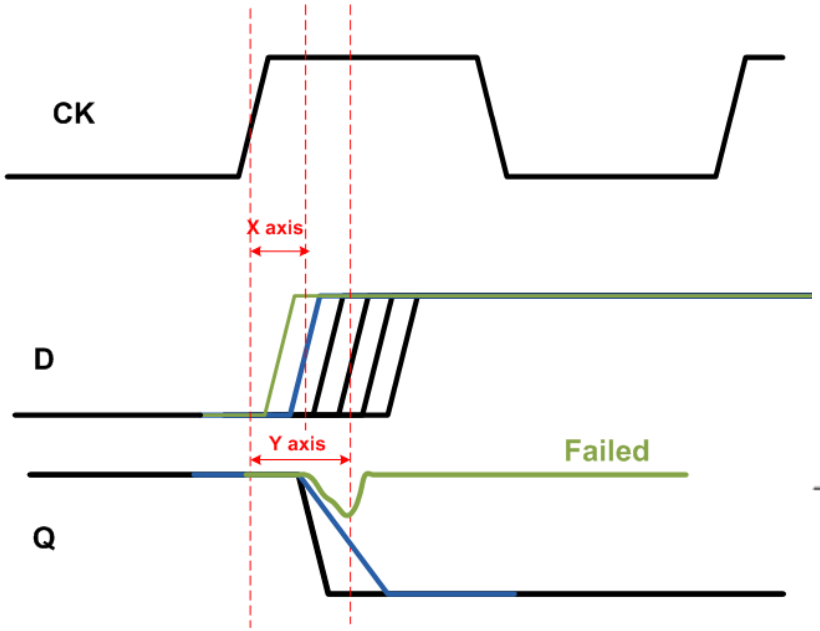


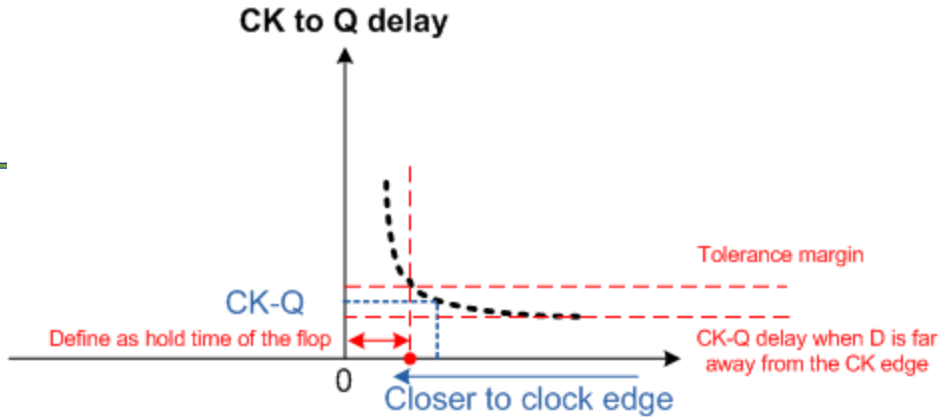


When D arrives after the setup time point, we call it setup time violation

Register (continue)

- Hold Time
- Input should be stable for a period of time after the clk edge





What do u need to notice in CAD2

1.Transmission gate direction

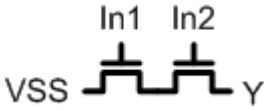
Remember the arrow of the transistor symbol means the direction of the current flow (see page 2 of tutorial 1.5)

2.Adding delay to the transistor in Verilog simulation

Adding delay to the left transistor will induce in1-to-Y delay

Adding delay to the right transistor will induce in2-to-Y delay

Adding delay to the both transistors?? You need to be careful about this.



3.Weak transistor

You need to use weak transistors (rpfet, rnfet) on the feedback path. In this example, using weak transistor on the transmission gate of the master latch, and the tri-state buffer of the slave latch.

4.How to measure the setup time/ hold time

Sweep the arrival time of the input, and set the margin to 5%, measuring the setup time and hold time

(The delay is measured between the 50% of amplitude of the signals)

Short key for Virtuoso

Adding geometries

Rectangle: r

Path: p

Label: l

Modifying geometries

Copy: c

Move: m (whole shape only)

Stretch: s (whole shape or edge)

Chop: shift + c

Merge: shift + m

Ruler

Create ruler: k

Delete all ruler: shift + k

Rotating and Flipping

After selecting copy , move, create instance, etc., HIT F3!

Hierarchy Edit

Descend edit: x

Return: b

Show all hierarchy: shift + f

Hide all hierarchy: ctrl + f

Create Instance: I

Other useful commands

Properties: q

Search: shift + s

Select all: ctrl + a

Deselect all: ctrl + d

Toggle on and off gravity: g

Redraw : ctrl + r

LSW

You can set the LSW to show only the layers that are in your layouts

[In Virtuoso Window] IBM_PDK->LSW->Present Layers Only

To add more layers that are not in the LSW

[In LSW Window] Edit->Set Valid Layers

CAD1

- Show me your layout and I can give you some advices.