

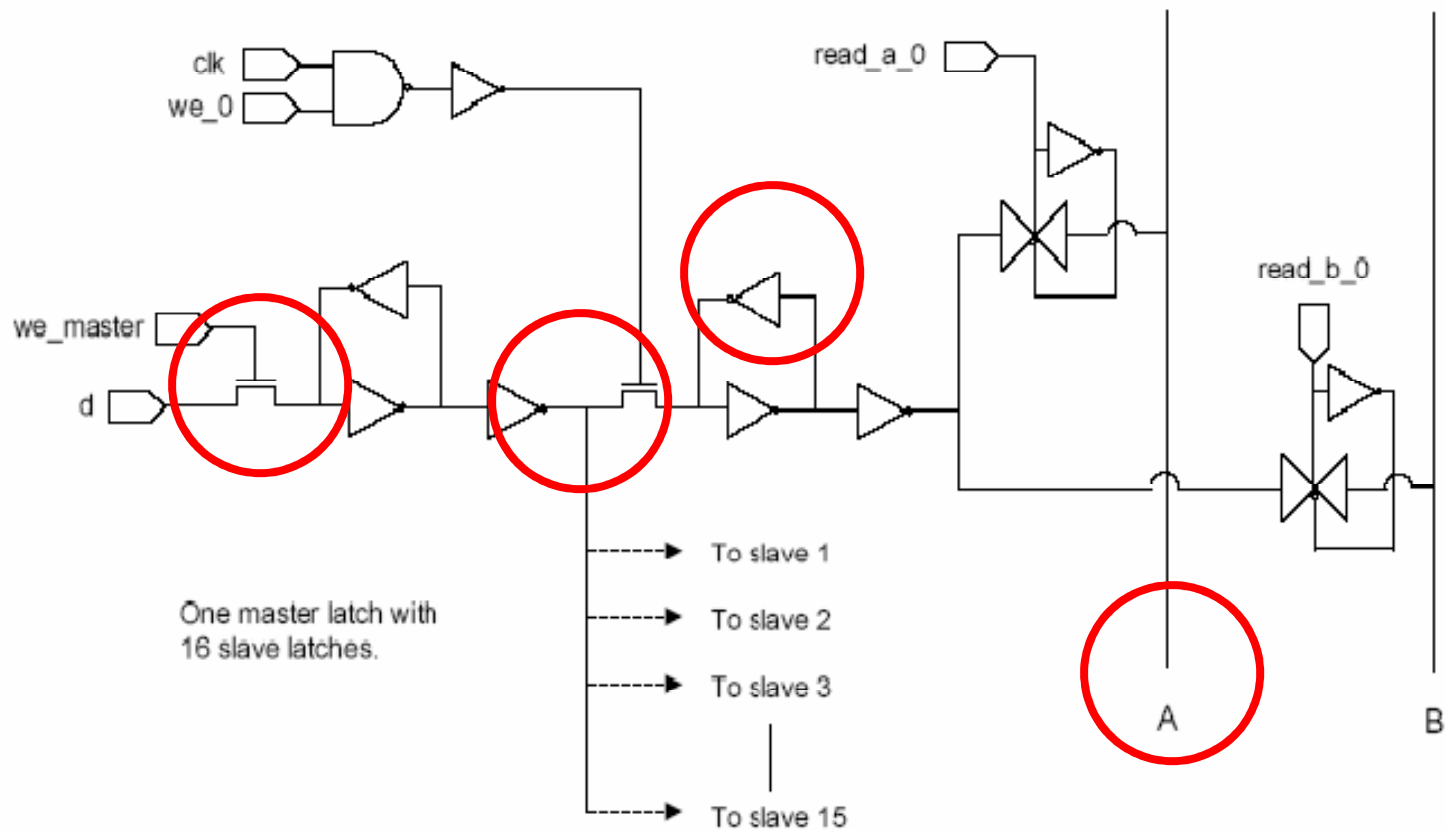
# CAD3 and more

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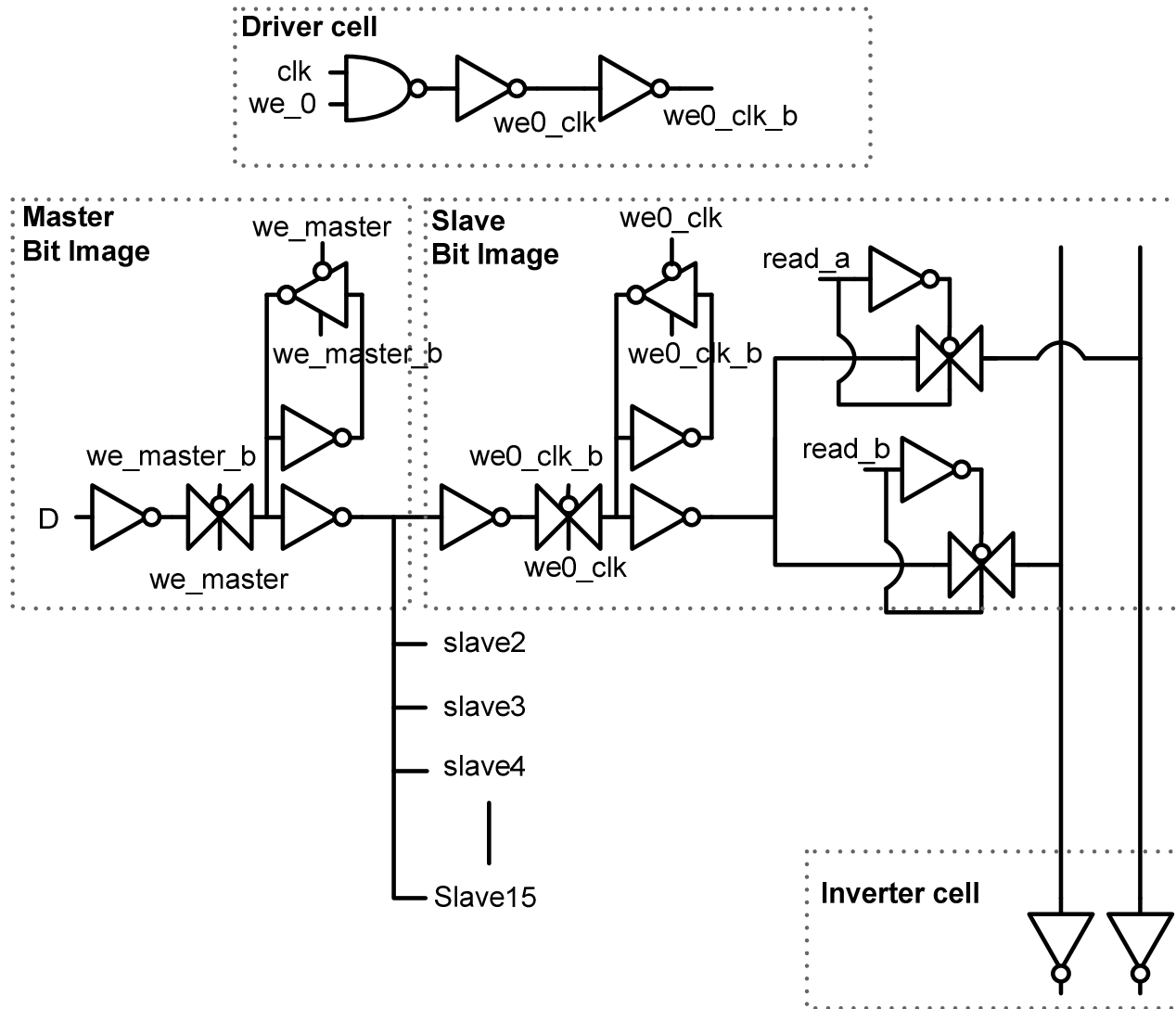
# CAD3

- Take advantage of the design hierarchy
- Use vector notation for both buses and instance
- The input and output signal polarity are not important.
- Reset is not required, but you should think about a way to reset your RF in the system.
- Speed-path simulation is a very important part of CAD3.
- Improve the density of your design.
- Use only M1-3

# RF Bit image



# Alternative RF Bit Image

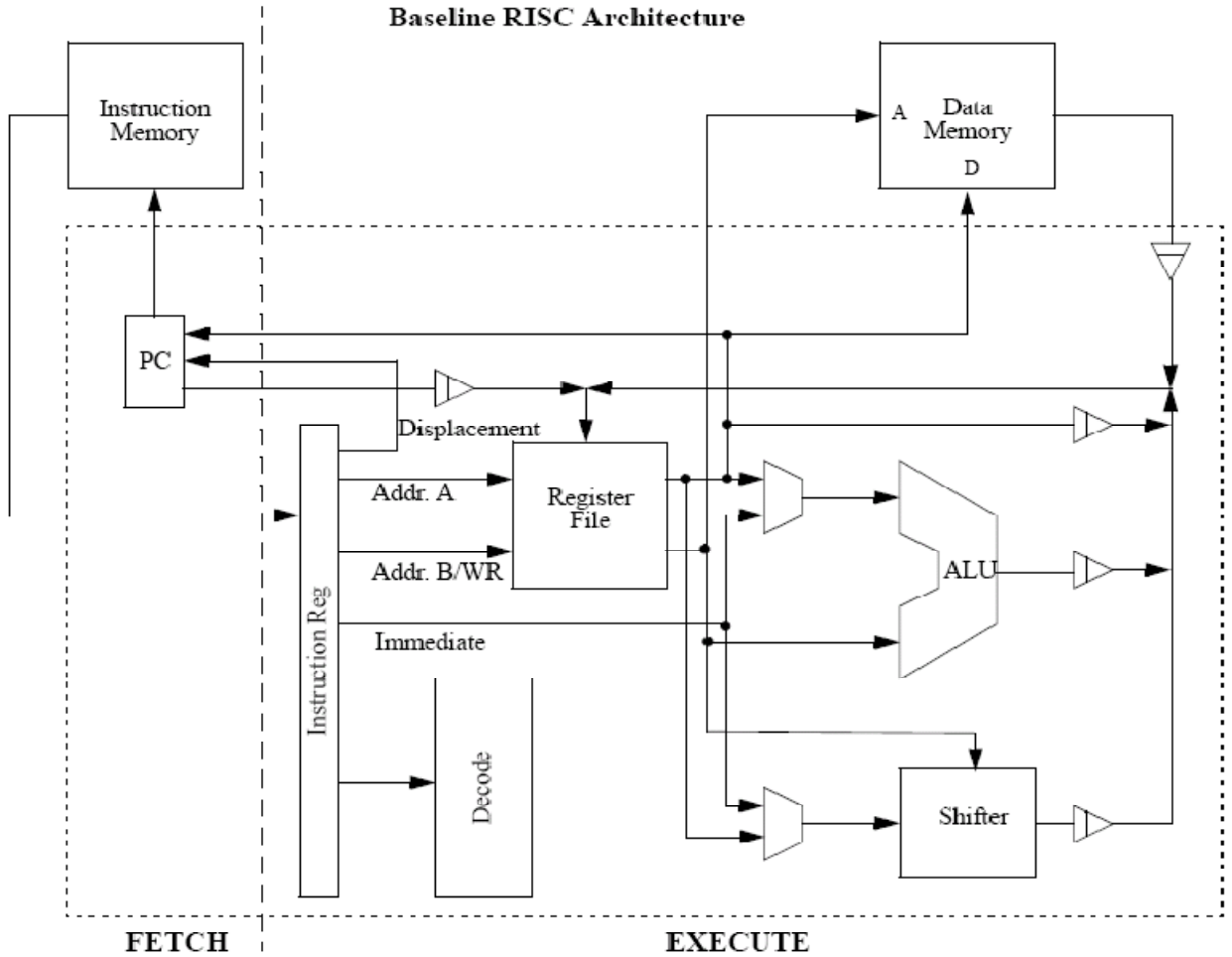




# EECS427 baseline ISA

- 16-bit RISC processor
- 2 stage pipeline: Fetch, Execute.
- Baseline ISA has a “\*” in the Notes.
- Decoder optimization table on page 3.

# Baseline RISC Architecture



# Importance of CAD3

- CAD3 set the bit width for your datapath.
- Be careful with your aspect ratio.
- Think about the connectivity between different blocks.

# Design with Hierarchy

- Hierarchy is good since it reduces the number of possible LVS errors.
- Adding additional hierarchy create overhead. (more pin, more schematic)
- Should design using True Hierarchy-> matching layout and schematic view.
- Try to create hierarchy to make the layout easier.

## Why do we need to maintain wiring track?

- Make sure that wiring track are consistent across different macros.
- It is easier to communicate with team member.
- Easier to plan your wire across different macros.