Discussion 4

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Announcement

• CAD3 is due today
• CAD4 will be online today
CAD4 requirements

- No metal4 and metal5 until datapath assignment
- Implement ADD, SUB, CMP, AND, OR, XOR, and immediate form of those functions
- Remember to implement the sign/zero extends
- Bit-slice width match with RF
- The VDD and GND metal2 power grid should use the same track as RF.
Logic functions

• 2 ways to implement the logic functions
  – Muxing: higher power, faster
  – Utilize part of the adder: lower power, slower.
    • Sum = A xor B xor C
    • Carry = AB + AC + BC

• XOR: output from sum, cin=0 for every bit
• AND: output from Cout, cin=0
• OR: output from Cout, cin=1
PSR
(Processor Status Register )

• Have signals ready for PSR
• PSR conditions: (Cn= carry out of MSB)
  – C: carry ( Cn for ADD, Cn_b for SUB)
  – F: overflow (Cn xor Cn-1)
  – Z: isZero (Nor bits of ALU output)
  – N: negative (Cn xor Cn-1 xor Sn-1) (signed)
  – L: low (Cn_b) (unsigned)
Future Discussion Topic

• CAD4 is ALU, CAD5 is shifter, both are custom project
• CAD6 is Program Counter (PC), and you need to use know Verilog /Synthesis flow to finish CAD6
• 2/13: Verilog/ Synthesis
• 2/20: Auto Place & Route (APR)
• Other suggestion??