Discussion 6

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Today

• Finish tutorial 2
Design Flow

**Configuration (*.conf)**
- Define cells and connectivity (*.v)
- Define layout for cells (*.lef)
- Define timing for cells (*.lib)
- Define timing constraints (*.sdc)

**Encounter Script (*.tcl)**
- Define io placement (*.io)
- Define floorplan area
- Define power ring/grid
- Define metal layer usage
- Define clock tree (not in this tutorial)

**SoC Encounter**

- (*.gds2), Import to icfb and get the layout
- (*.apr.v), Import to icfb and get the schematic
- (*.apr.sdf), delay information, post-layout verilog simulation
- (*.lef), layout abstract, include this fine when doing top-level integration
Demo

- Standard cells
- mult.conf (configuration)
- mult.tcl (command script)
- Import *gds2, *apr.v
- DRC, LVS
- Post-layout verilog simulation
more...

- March 6\textsuperscript{th} is the last discussion, and I will go through tutorial 2.5 (top-level integration) during the discussion.

Have a nice spring break!