Discussion 7

Wei-Hsiang Ma

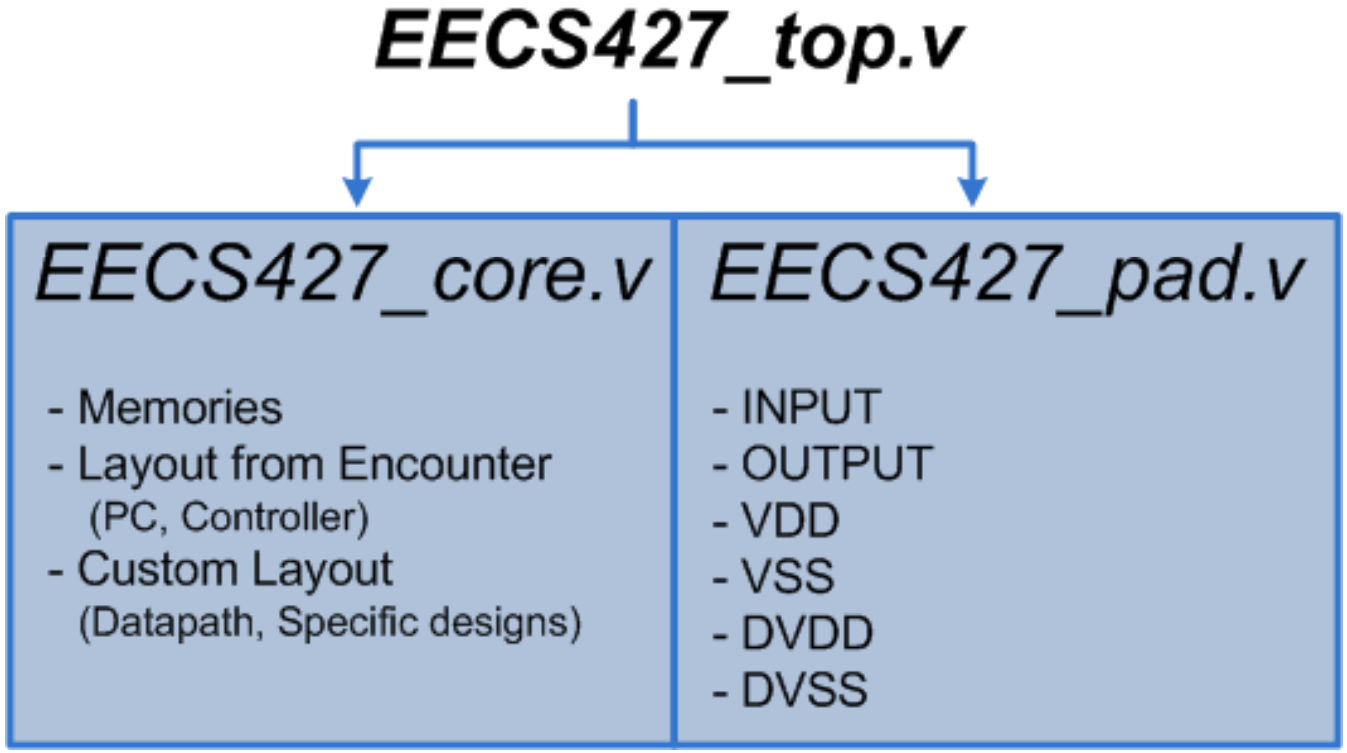
2009/03/06

Today

- Tutorial 2.5 (Integration Tutorial)

- Integrate everything together: memories, layout from Encounter, and layout from your CAD assignments.

Design Hierarchy

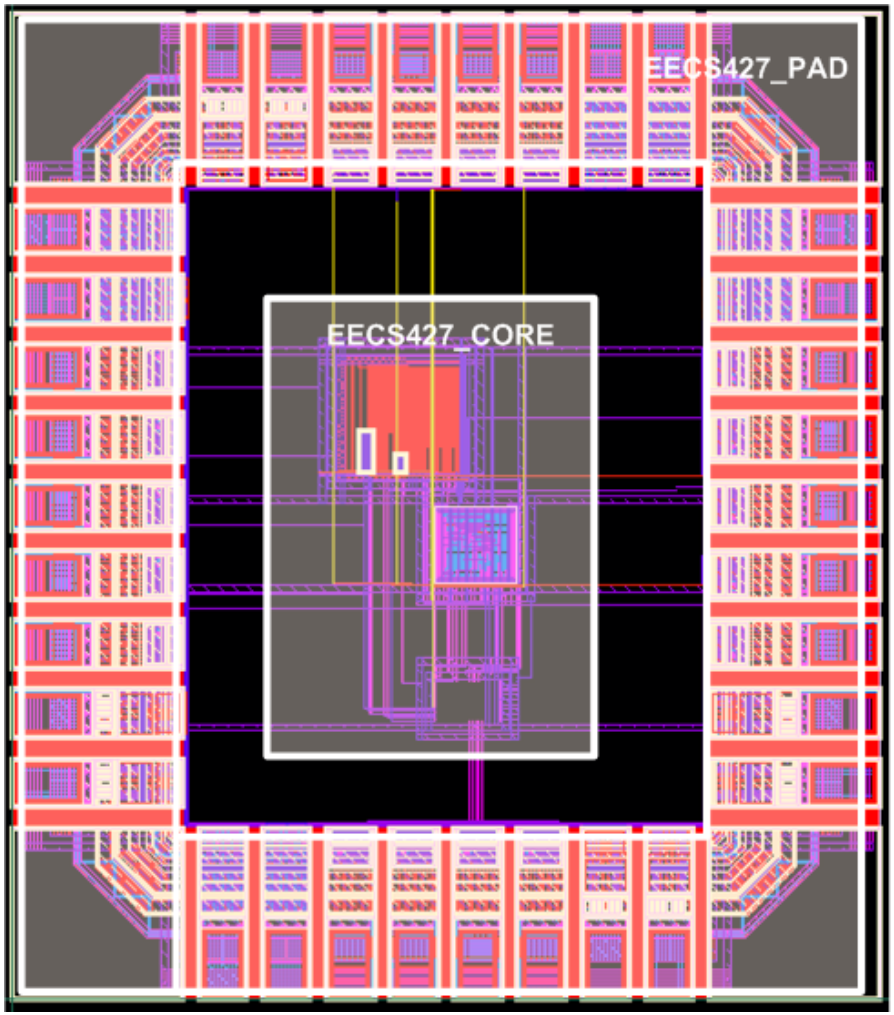


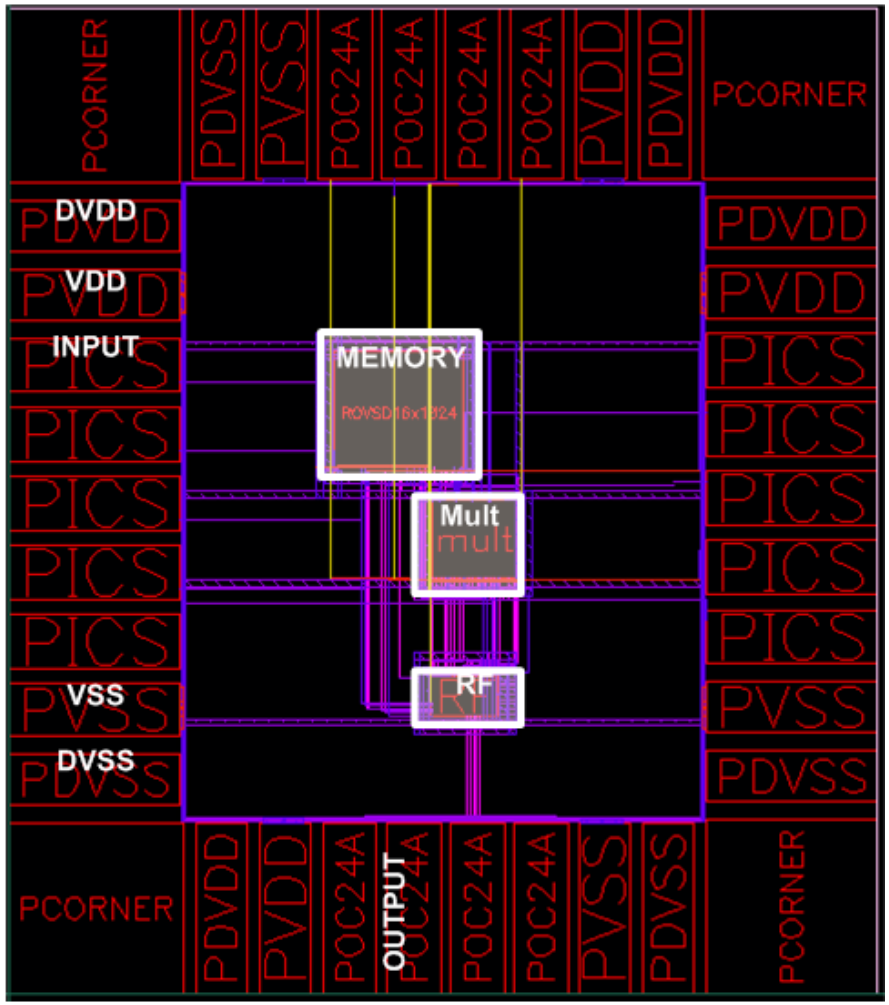
Dirty VDD, Dirty VSS

- Dirty VDD (DVDD) is a power supply to communicate with outside world.
  - DVDD has more noise.
  - DVDD is usually larger than VDD.

- Dirty VSS (DVSS) should be separated from VSS to avoid noise issue.

Layout


EECS427_PAD
EECS427_CORE


PCORNER
PDVSS
PVSS
POC24A
POC24A
POC24A
POC24A
PVDD
PDVDD
PCORNER
DVDD
VDD
INPUT
MEMORY
ROVSD16x1924
Mult
mult
RF
VSS
DVSS
PCORNER
PDVDD
PVDD
POC24A
OUTPUT
POC24A
POC24A
POC24A
PVSS
PDVSS
PCORNER

What do you need before integration?

- Decide which memory you want to use
- *.lef and *.apr.v after Encounter
- *.lef and *.v for your custom layout
- A verilog file that has the connectivity of all blocks (without pads)
- The order for your I/O pads

For your custom designs

- *How to make a verilog file for your custom designs?*

  A: Make an empty module with all inputs, and outputs (you don't have to include VDD, VSS).

- *How to make a lef file for your custom designs?*

  A: I will make that for you. I have an example in LEF_EXAMPLE. Please modified your layout before you send it me.

Demo

- LEF_EXAMPLE
- EECS427_CORE.v (Define the connectivity)
- EECS427_TOP.raw (Define the I/O pads)
- Encounter
- Stream in, Verilog in,
- Fix DRC.
- Add DVDD, DVSS labels and pass LVS.

This is the last discussion

Good luck!