

EECS 427: VLSI Design I
 Winter 2009 Syllabus, Revised 1/7/09

Texts: Default = Rabaey, WH = Weste and Harris, CBF = Chandrakasan, Bowhill, and Fox

Date	Topic	Reading/Coverage	Notes, assignments due
January 8	Manufacturing, intro	1.1-1.3 (review), 2.2, WH 3.2	
1/13	Design rules & layout	2.3, insert A, WH 1.5, WH 3.3	CAD tutorial, 1/13 7-9pm 1620 East CSE HW 1 due 1/16 5pm
1/15	Design flows	8.1-8.4	CAD 1 due 1/19
1/20	CMOS review (Sylvester OUT)	5.4, 5.5, 6.2, 6.3	
1/22	Interconnect review (Sylvester OUT)	4.3, 9.2, 9.3	CAD 2 due 1/26
1/27	Project architecture and LE	Notes	HW2 due in class (teams)
1/29	Logical effort	Notes	
February 3	Logical effort, adders	11.1-11.3.1	
2/5	Adders	11.3.2-11.3.3	CAD 3 due 2/6
2/10	Multipliers (Sylvester OUT)	11.4	HW 3 due in class (initial proposal)
2/12	Shifters	11.5, WH 10.8	
2/17	Low-power ALUs	11.7	CAD 4 due 2/17
2/19	Quiz 1		
2/24, 2/26, no classes, spring break			
March 3	Counters, pipelining	WH 10.5, notes	CAD 5 due 3/3
3/5	Timing, skew/jitter	10.1-10.3	HW4 due in class (detailed proposal)
3/10	Continue timing, D-Q, pulsed latches (Sylvester OUT)	10.3, 7.4	CAD 6 due 3/10
3/12	Design for test	Insert H.3, CBF Ch. 25	
3/17	Synthesis/APR flow	Notes, WH 8.4	
3/19	Verilog overview	Notes, WH Appendix A	HW 5 due 3/19
3/24	Memory core and peripherals	12.2, 12.3	CAD 7 due 3/24
3/26	Memory reliability and power	12.4, 12.5	
3/31	System-level power reduction techniques	6.4.2, CBF Ch. 4	
April 2	Clock distribution (Sylvester OUT)	10.3.3, 10.6, CBF Ch. 13	
4/7	Advanced interconnect	9.5	
4/9	Power distribution	WH 12.3, CBF Ch. 24	CAD 8 due 4/9
4/14	Advanced topics/overflow	Notes	
4/16	Quiz 2		
4/21	Project Presentations		HW 6: Presentations
4/24	Final Project Demos		Final reports due 4/27, noon

Summary of *tentative* due dates:

HW1 (problem set): Friday Jan 16 @5pm, to Nicole Frizzell in 2417 EECS

HW2 (teams): Tuesday Jan 27, in class

HW3 (initial proposal): Tuesday Feb 10, in class

HW4 (detailed proposal): Thursday Mar 5, in class

HW5 (external interfaces): Thursday Mar 19, in class

HW6 (project presentations): Tuesday Apr 21, in class

All CADs due at 7pm except CAD9.

CAD1 (inverter/nand/mux): Monday, Jan 19

CAD2 (D flip-flop): Monday, Jan 26

CAD3 (register file): Friday, Feb 6

CAD4 (ALU): Tuesday, Feb 17

CAD5 (shifter): Tuesday, Mar 3

CAD6 (program counter): Tuesday, Mar 10

CAD7 (datapath): Tuesday, Mar 24

CAD8 (controller): Thursday, Apr 9

CAD9 (project completion/demo): Friday, Apr 24