EECS 427
Winter 2009
HW1 (review)
Relevant sections to review: 3.3.2, 5.3, 5.4, 6.2, 7.1.1, 7.2.3
**Due: Friday Jan. 16th 5pm to Nicole Frizzell, 2417 EECS**

Default technology: the minimum drawn channel length = 0.25um, the effective channel length for $L_{drawn}$ of 0.25um is 0.2um, nominal $V_{dd}$=2.5V, see table "CMOS (0.25um) – Unified Model" on inside back cover of Rabaey for other parameters.

Unless otherwise specified assume that the junction capacitance of a MOSFET is equal to half of its gate-to-channel capacitance $C_{gc}$ (i.e., $C_{db} = C_{sb} = C_{gc}/2$). Ignore overlap capacitances. Assume cutoff region when computing gate capacitance (Table 3-4) and note that the relevant channel length term for the capacitor area is the effective channel length.

1. In a CMOS inverter with minimum channel length transistors and $W_n$=1um:
   **a).** Find $W_p$ such that $V_M \leq 1V$ and $t_{plh}$ is minimized.
   **b).** Also, find $t_{plh}$ in this case when the total output capacitance is 10fF. Refer to Table 3.3 of Rabaey (pg. 106) to help in computing delay. However, make the change that the table entries are for W=0.25um and $L_{eff}$=0.2um. Ex: for $V_{dd}$=1V and $W_n$=0.5um, $R_{eq}$ = 35kΩ/(0.5/0.25) = 17.5kΩ. In Equation 5.3 of Rabaey, $r = k_p*V_{dsatp} / k_n*V_{dsatn}$ but is NOT equal to $v_{satp}*W_p/v_{satn}*W_n$.

2. **a).** Implement equation $Y=\overline{(A \cdot B + B \cdot C + A \cdot C)}$ in a CMOS gate.
   **b).** Size the devices so that the output resistance is the same as that of an inverter with $W_n$ = 0.5um and $W_p$ = 1.5um.
   **c).** Write the Boolean expression for the function performed by the circuit given in Fig. 1
   **d).** Compare the circuits in 2.a, and Fig. 1, and list at least one advantage for Fig. 1 over 2.a.

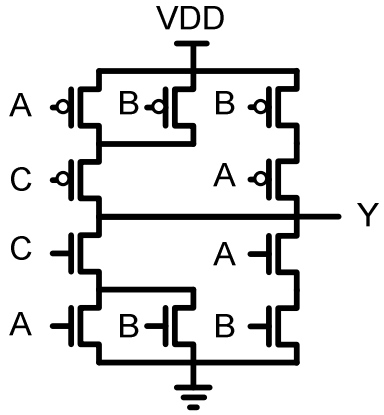

Figure 1

3. Consider the combinational circuit shown in Fig. 2. The probability of all the primary inputs of the circuit to be in either state '0' or state '1' in a clock cycle is 0.5 (i.e. Pni(0)=Pni(1)=0.5 for i = 0,1,2). The probability of switching of any primary input in a clock cycle is 0.1 (i.e. Pn0(sw)=Pn1(sw)=Pn2(sw)=0.1). Compute the average dynamic power dissipation of the circuit at 500MHz and 1GHz. For simplicity, assume that the total capacitive load at any net ni (i = 0, 1, 2, 3, 4) in the circuit is 10fF (ignore any other capacitances). Assume that all the primary inputs are spatially as well as temporally uncorrelated.

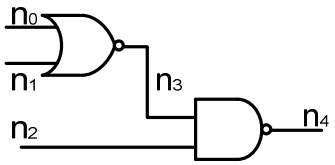


Figure 2

4. Consider the static CMOS NAND gate shown in Fig. 3. Ignoring junction leakage and subthreshold current, determine the voltage of node n and the threshold voltage of transistor A and transistor B.

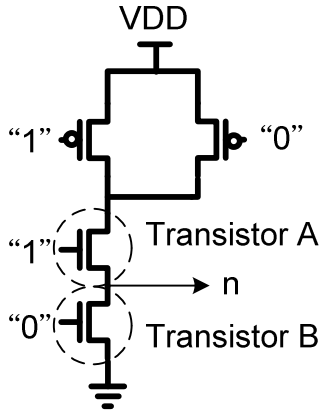


Figure 3

5. See Fig. 4 for a timing diagram of a positive edge-triggered register with data input A, B and output Q. Draw the corresponding D and Q waveform given the relevant timing information for setup and hold times and clock-q delay. Please mark times at which either the setup or hold time are violated. Assume Q is initially low. ($T_{CLK-Q}$ = 3 units, $T_{setup}$ = $T_{hold}$ = 2 units, $T_{nand}$=2units)

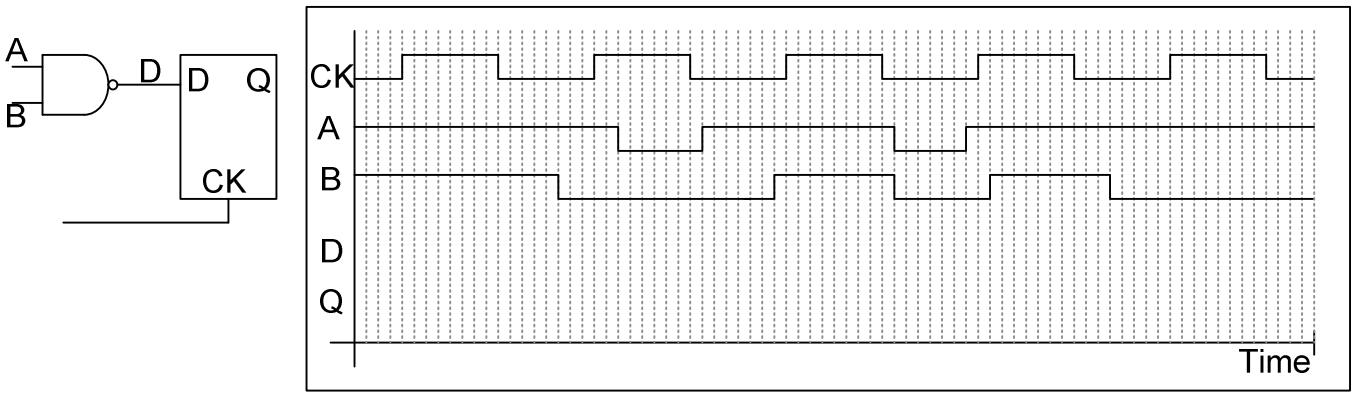


Figure 4