1. In a CMOS inverter with minimum channel length transistors and $W_n=1\mu m$:

   a). Find $W_p$ such that $V_M \leq 1V$ and $t_{plh}$ is minimized.
   b). Also, find $t_{plh}$ in this case when the total output capacitance is 10fF. Refer to Table 3.3 of Rabaey (pg. 106) to help in computing delay. However, make the change that the table entries are for $W=0.25\mu m$ and $L_{eff}=0.2\mu m$. Ex: for $V_{dd}=1V$ and $W=0.5\mu m$, $R_{eq}=35K\Omega/(0.5/0.25)=17.5K\Omega$. In Equation 5.3 of Rabaey, $r = k_p^*V_{dsatp}/k_n^*V_{dsatn}$ but is NOT equal to $v_{satp}^*W_p/v_{satn}^*W_n$.

   

   $V_M \leq 1V$ , $W_p$ small leads to low $V_M$

   $t_{plh}$ minimized, $W_p$ big lead to small $t_{plh}$

   So, we are looking for $V_M=1V$

   a)

   $V_M = \left( V_{thn} + \frac{V_{dsatn}}{2} \right) + \sqrt{V_{DD} + V_{thp} + \frac{V_{dsatp}}{2}} \right) \div \left( 1 + \gamma \right)$

   $\gamma = \frac{k_p^*V_{dsatp}}{k_n^*V_{dsatn}} = \frac{3.01W_p}{115.63W_n} = 0.414W_p \ (W_p \ in \ \mu m)$

   Use above two equations and get $W_p=1.03\mu m$

   b)

   $t_{plh} = 0.69R_{eq}C_L$

   $R_{eq} = \frac{31K\Omega (table=3-3)}{1.03/0.25} = 7.52K\Omega$

   $t_{plh} = 51.92ps$
2. **a)** Implement equation \( Y = (A \cdot B + B \cdot C + A \cdot C) \) in a CMOS gate.  
**b)** Size the devices so that the output resistance is the same as that of an inverter with \( W_n = 0.5\mu m \) and \( W_p = 1.5\mu m \).  
**c)** Write the Boolean expression for the function performed by the circuit given in Fig. 1.  
**d)** Compare the circuits in 2.a, and Fig. 1, and list at least one advantage for Fig. 1 over 2.a.

(a), (b)

![Circuit Diagram](image)

(c), \( Y = (A \cdot B + B \cdot C + A \cdot C) \)  
(d) Small total transistor size with the same driving ability, smaller size layout possible. Easier for layout since PDN and PUN are symmetric.

3. Consider the combinational circuit shown in Fig. 2. The probability of all the primary inputs of the circuit to be neither state '0' or state '1' in a clock cycle is 0.5 (i.e. \( P_{n0}(0)=P_{n1}(1)=0.5 \) for \( i = 0, 1, 2 \)). The probability of switching of any primary input in a clock cycle is 0.1 (i.e. \( P_{n0}(sw)=P_{n1}(sw)=P_{n2}(sw)=0.1 \)). Compute the average dynamic power dissipation of the circuit at 500MHz and 1GHz. For simplicity, assume that the total capacitive load at any net \( n_i \) (\( i = 0, 1, 2, 3, 4 \)) in the circuit is 10fF (ignore any other capacitances). Assume that all the primary inputs are spatially as well as temporally uncorrelated.

![Circuit Diagram](image)
3. Sol:

![Logic Diagram]

We only care about 0 → 1 transitions. \( P_{dyn} = C_L V_{DD}^2 f \times D \)

\[
P_{n1,0\rightarrow1} = 0.5 \times 0.1 = 0.05
\]

\[
P_{n2,0\rightarrow1} = 0.5 \times 0.1 = 0.05
\]

\[
P_{n3,0\rightarrow1}:
\begin{array}{c|ccc}
0 & 0 & 1 & 1 \\
0 & 0 & 0 & 1 \\
1 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 \\
\end{array}
\]

\[
P(0,0) \rightarrow P(0,0) = \frac{1}{4} \times 0.1 \times 0.9
\]

\[
P(1,0) \rightarrow P(0,0) = \frac{1}{4} \times 0.1 \times 0.9
\]

\[
P(1,1) \rightarrow P(0,0) = \frac{1}{4} \times 0.1 \times 0.9
\]

\[
P_{n4,0\rightarrow1}:
\begin{array}{c|ccc}
0 & 0 & 1 & 1 \\
0 & 0 & 0 & 1 \\
1 & 1 & 1 & 1 \\
1 & 1 & 0 & 0 \\
\end{array}
\]

\[
P_{n3,1\rightarrow0} = P(0,0,1) \times 0.9 = 0.9 \times 0.9
\]

\[
P(n_0, n_1, 00 \rightarrow 01) = 0.9 \times 0.1
\]

\[
P(n_0, n_1, 10 \rightarrow 10) = 0.1 \times 0.9
\]

\[
P(n_0, n_1, 00 \rightarrow 11) = 0.1 \times 0.1
\]

\[
P_{n4,0\rightarrow1} = \frac{1}{8} (0.081 + 0.19)
\]

\[
= 0.034
\]

\[
P_{dyn} = 0.05 + 0.05 + 0.05 + 0.0475 + 0.034 \times 10^4 \times (2.5)^2 \times f
\]

\[
f_{GHz} = 14.47 \text{GHz}
\]

\[
s_{MHz} = 7.23 \text{MHz}
\]
4. Consider the static CMOS nand gate shown in Fig. 3. Ignoring junction leakage and subthreshold current, determine the voltage of node n and the threshold voltage of transistor A and transistor B.

The voltage at node n is the solution to the equation

\[ V = V_{dd} - (V_{th} + \gamma(\sqrt{V + 0.6} - \sqrt{0.6})) \]

\[ V = 2.5 - (0.43 + \gamma(\sqrt{0.6} - \sqrt{0.6})) \]

Solving the equation gives \( V = 1.76 \text{V} \)

\[ V_{th,A} = 0.43 + \gamma((1.76 + 0.6)^{0.5} - (0.6)^{0.5}) = 0.735 \text{V} \]

\[ V_{th,B} = 0.43 + \gamma((0 + 0.6)^{0.5} - (0.6)^{0.5}) = 0.430 \text{V} \]

5. See Fig. 4 for a timing diagram of a positive edge-triggered register with data input A, B and output Q. Draw the corresponding D and Q waveform given the relevant timing information for setup and hold times and clock-q delay. Please mark times at which either the setup or hold time are violated. Assume Q is initially low. (\( T_{\text{CLK-Q}} = 3 \text{ units}, T_{\text{setup}} = T_{\text{hold}} = 2 \text{ units}, T_{\text{nand}} = 2 \text{ units} \))