EECS 427
VLSI Design I

TuTh 9-10:30am
Disc: F 4:30-5:30
Prof. Dennis Sylvester

http://www.eecs.umich.edu/courses/eecs427

Outline

- Logistics – teaching staff intro, go over syllabus
- What I expect you to learn in this class
- CMOS processing sequence

Teaching Staff

- Primary instructor: myself (dennis@eecs.umich.edu)
- GSIs:
  - Wei-Hsiang Ma (wsma@umich.edu)
    - 427 lead GSI: covers lecture material + project, leads discussion, software tools
    - ALSO 627 GSI
  - Jae-Sun Seo (jseo@umich.edu)
    - 627 lead GSI, ALSO covers 427 in office hours
    - Mainly to help with tool/project issues
- Staff support:
  - Joel Van Laven (jvanlav@umich.edu)
    - Major CAD tool issues (pertaining to the project); consult *after* Wei-Hsiang and Jae-Sun

Course setup

- Tues and Thur lectures in 1003 EECS
- Friday discussion section led by Wei-Hsiang (1003 EECS)
  - Purpose of discussion: review lecture topics, answer common questions regarding CAD assignments
- Homeworks
  - Only 1 'typical' HW, others handle planning issues of project (groups, initial proposal, etc.)
- CAD assignments
  - Roughly weekly, several 2-week assignments
  - Each assignment represents a component of your final microprocessor design
  - First 2 are individual, rest are in groups
  - Tutorial: Tuesday 1/13, 7-9pm, 1620 CSE (to be confirmed)
- Will try out a course wiki this semester (Ctools)

Project

- Main component of class, 70+% of your grade
- Design a 16-bit RISC (reduced instruction set computing) processor
  - Groups of 4 (you choose)
    - Good to have a mix of EE and CE so there is some architecture background in your group
  - Baseline architecture (instruction set) given to you; you choose an application and add a few peripherals
  - Time requirements: 30-40 hrs/week avg.
  - Peer contribution forms; must pull your weight
- Learn full-custom design (datapath) and design automation tools (logic synthesis + automated place/route for control logic)
- You can send this design off to be fabricated and test it later as a directed study or possibly in EECS 579 (encouraged!)

Logistics

- Course Textbook:
  Digital Integrated Circuits: A Design Perspective, 2nd edition by Rabaey, Chandrakasan, and Nikolic
- Lecture notes will be posted online shortly before class sessions and I will bring copies to class for note taking
- I will supplement this book with several handouts from other sources throughout the semester
- Other books on reserve at Media Union (Weste, Chandrakasan, Hodges, and Franzon)
  - Weste/Harris in particular is recommended if you want to pursue a career/graduate studies in digital circuits
- Get on class email list
  - Send blank email to eecs427-request@eecs.umich.edu with "subscribe" as subject – should get confirmation email

Grade Breakdown

- Your project, in the form of CADs and final report/presentation, is the dominant part of your grade

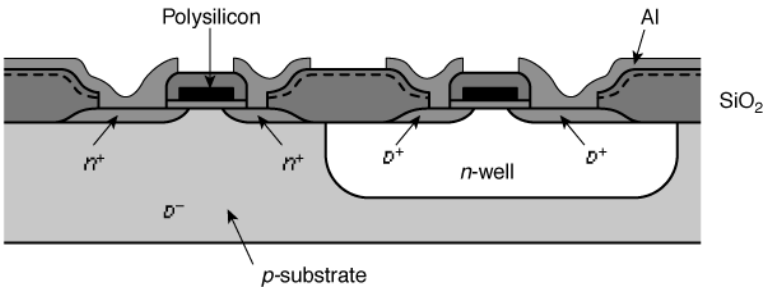
Homework	10%
CAD assignments	35%
Quizzes	24% (12% each)
Final project/report, indiv. contrib.	31%

CAD late policy: within 24 hours = 25% penalty, 24-48 hours = 50% penalty, see course info handout

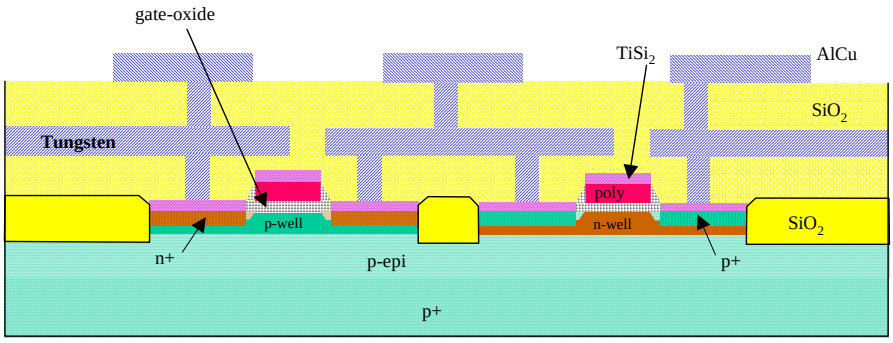
What you will learn in this class

- The entire process of very large-scale digital design
  - Custom integrated circuit layout
  - Sub-system design such as adders, register files, program counters, etc.
  - Synthesis + automated place/route design flow
  - **Teamwork**
- Advanced circuit design topics such as:
  - Multipliers, pulsed latches, memory decoder and sense amplifiers, etc.

CMOS Process

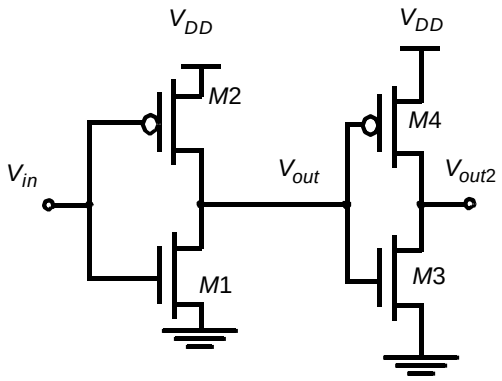


A Modern CMOS Process

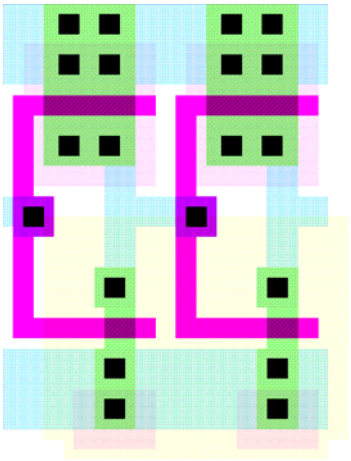


Dual-Well Trench-Isolated CMOS Process

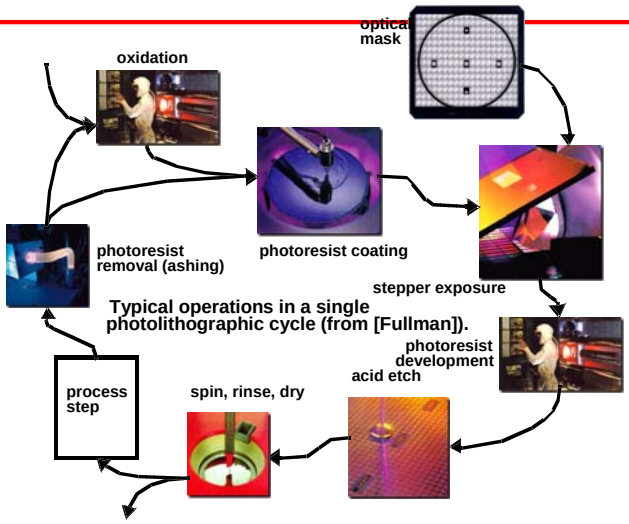
Circuit Under Design



Its Layout View

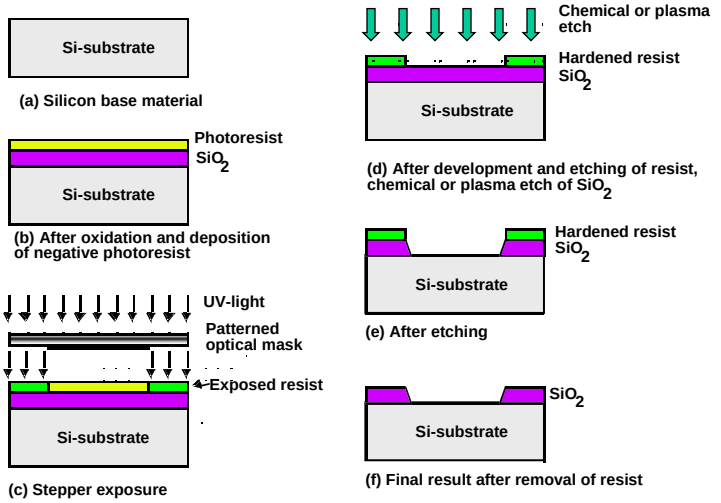


Photolithographic Process

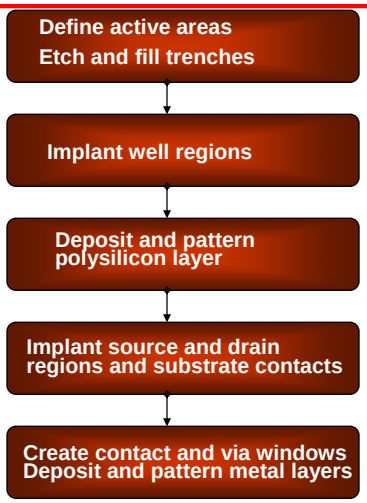


Typical operations in a single photolithographic cycle (from [Fullman]).

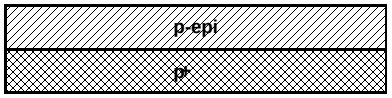
Patterning of SiO_2



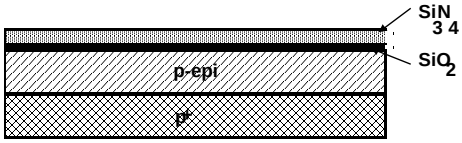
CMOS Process at a Glance



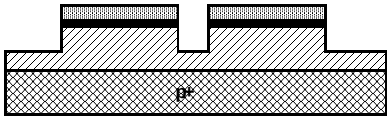
CMOS Process Walkthrough



(a) Base material: p+ substrate with p-epi layer

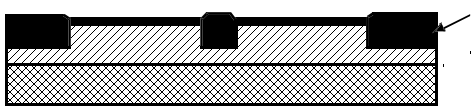


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

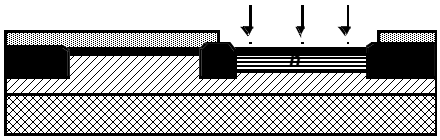


(c) After plasma etch of insulating trenches using the inverse of the active area mask

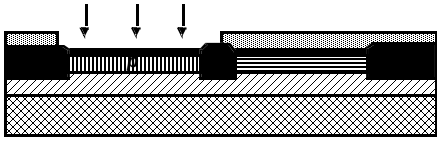
CMOS Process Walkthrough



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

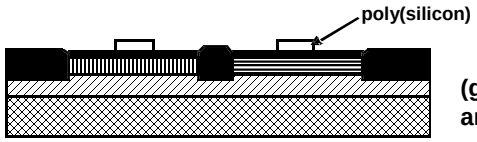


(e) After n-well and Vthp adjust implants

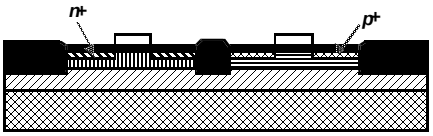


(e) After p-well and Vthn adjust implants

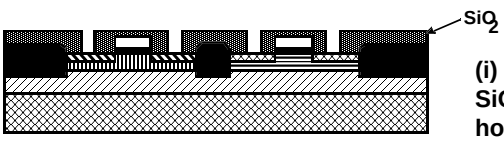
CMOS Process Walkthrough



(g) After polysilicon deposition and etch

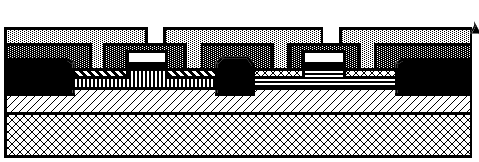


(h) After n+ source/drain and p+ source/drain implants. These steps also dope poly.

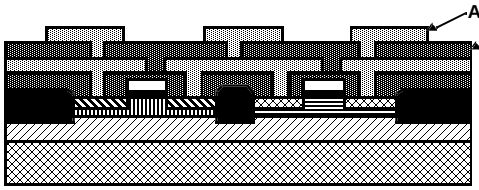


(i) After deposition of SiO2 insulator and contact hole etch

CMOS Process Walkthrough



(j) After deposition and patterning of first Al layer.



(e) After deposition of SiO_2 Insulator, etching of vias, deposition and patterning of 2^{nd} layer of Al

Looking Ahead

- http://jas.eng.buffalo.edu/education/fab/invFab/index.html
- Read Sections 1.1, 1.2, 1.3.2-1.3.4, and 2.2 of Rabaey (mostly review)
- We'll cover design rules and layout styles, then briefly review CMOS and interconnect analysis
- Then
  - Logical effort
  - ALU operations (add/shift/multiply)
  - Timing (skew/D-Q delay plots/clocking)
  - Memory, design-for-test, clock distribution…