EECS 427
Lecture 13: Timing
Reading: 10.1 – 10.2

Last Time

- Use of 2 Vdd’s on a chip is growing
  - Brings up level conversion, layout, power distribution issues
- Fast, energy efficient level converter topologies are critical to maximize dual-Vdd benefit
Lecture Overview

- Exam 1:
  - M = xxx
  - X = yyy
- Skew/jitter & other timing definitions

Synchronous Timing

```
CLK
  In
  R1  Combinational Logic  R2
  Out
```
**Latch Parameters**

Delays can be different for rising and falling data transitions.

**Register (FF) Parameters**

Delays can be different for rising and falling data transitions.
Clock Waveform Nonidealities

- **Clock skew**
  - Spatial variation in temporally equivalent clock edges, $\delta$

- **Clock jitter**
  - Temporal variations in consecutive edges of the clock signal
    - Cycle-to-cycle (short-term) $t_{JS}$
    - Long term $t_{JL}$

- **Variation of the pulse width (duty cycle)**
  - Important for level-sensitive (latch-based) clocking

Clock Skew and Jitter

- Both skew and jitter impact the effective cycle time
Idealized View of Clock Skew

Earliest occurrence of Clk edge
Nominal − δ/2

Latest occurrence of Clk edge
Nominal + δ/2

Max Clk skew

δ

IBM microprocessor clock skew

# of paths
Positive and Negative Skew

(a) Positive skew

(b) Negative skew

Positive Skew, $\delta > 0$

Launching edge arrives before the receiving edge
Good for performance, bad for hold time
Key: Hold time violations cannot be fixed by running the clock slower!
Negative Skew, $\delta < 0$

Receiving edge arrives before the launching edge
Bad for performance, good for hold time violations

Timing Constraints

Minimum cycle time:
$T \geq t_{c-q} + t_{su} + t_{logic} - \delta$

Worst case is when receiving edge arrives early (negative $\delta$)
**Timing Constraints**

- **In**: \( R1 \) → \( D \) → \( Q \) → \( R2 \)
- **CLK**: \( t_{CLK1} \) → \( t_{CLK2} \)
- **\( t_{c-q} \)**
- **\( t_{c-q, cd} \)**
- **\( t_{su, thold} \)**
- **\( t_{logic} \)**
- **\( t_{logic, cd} \)**

**Hold time constraint:**

\[
t_{(c-q, cd)} + t_{(logic, cd)} > t_{hold} + \delta
\]

Worst case is when receiving edge arrives late (positive skew)
Race between data and clock
\( cd \): contamination delay (fastest possible delay)

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**Impact of Jitter**

- 3-4: shortened clock period
Longest Logic Path in Edge-Triggered Systems

If launching edge is late and receiving edge is early, the data will not be too late if:

\[ T_{c-q} + T_{logic} + T_{su} < T - T_{JS,1} - T_{JS,2} + \delta \]

Minimum cycle time is determined by the maximum delays through the logic

\[ T_{c-q} + T_{LM} + T_{SU} - \delta + 2 T_J < T \]
Jitter Sources

• Caused by variations in clock period that result from:
  – Phased-lock loop (PLL) oscillation frequency
  – Various noise sources affecting clock generation and distribution
    • Ex. Power supply noise which dynamically alters the drive strength of intermediate buffer stages

Latch vs. Flip-Flop Timing

• 2-phase clocking for latches
  – Skew tolerance
  – Difficult to generate
  – Good for high performance designs (e.g., custom microprocessors)
  – Timing verification more complex

From Weste/Harris
Time Borrowing

- In a flop-based system:
  - Data launches on one rising edge
  - Must setup before next rising edge
  - If it arrives late, system fails
  - If it arrives early, time is wasted
  - Flops have hard edges

- In a latch-based system:
  - Data can pass through latch while transparent
  - Long cycle of logic can borrow time into next
  - As long as each loop completes in one cycle

Time Borrowing Example

Loops may borrow time internally but must complete within the cycle.
Summary

• Clocks strongly impact IC performance (timing) and are not ideal
  – Skew and jitter are commonly discussed non-idealities
  – Skew is typically larger and more heavily focused on
  – More on skew later in class when we discuss clock distribution techniques
• Rough rule of thumb: skew should be kept < 10% of clock period