EECS 427
Lecture 14/15: Timing/Latch Design
Reading: 10.3.1, 10.3.2, 7.4.1

Last Time

- Defining skew, jitter
  - Sources
- Impact on minimum cycle time
- Time borrowing
  - Possible in latch-based systems, not edge-triggered registers
  - Improves performance

Lecture Overview

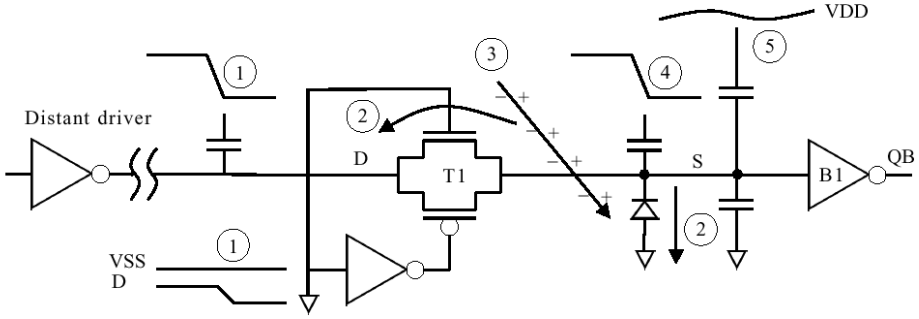
- Noise sources relevant to FFs
- Description of the D-Q delay of FFs
- Pulsed registers

Requirements in Flip-Flop Design

- High speed:
  - Small Clk-Output delay
  - Small setup time
  - Small hold time→Inherent race immunity
- Low power
- Small clock load (clock power is very large)
- High driving capability
- Integration of the logic into flip-flop
- Multiplexed or clock scan (testability)
- Robustness
- Crosstalk insensitivity
  - Dynamic/high impedance nodes are affected

Sources of Noise

1. Noise on input
2. Leakage
3. α-Particle and cosmic rays
4. Unrelated signal coupling
5. Power supply ripple



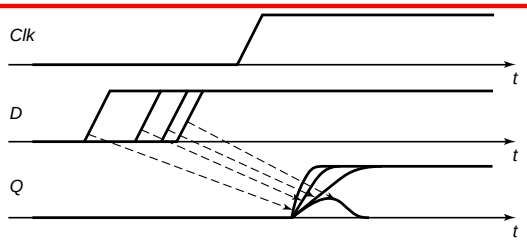
Flip-Flop Robustness

- Input isolation
  - Don't use a pass-transistor directly at the input (use a buffer)

Storage node related issues:

- Robustness
  - No floating nodes, create pseudo-static storage nodes
- Min capacitance limit
  - Storage node (middle of cross-couple) should have a decent amount of capacitance for noise immunity
  - Too much will slow things down though…
- Preventing exposure
  - Wires associated with storage node should be short, suppress possible coupling to other nodes

More Precise Setup Time Definition

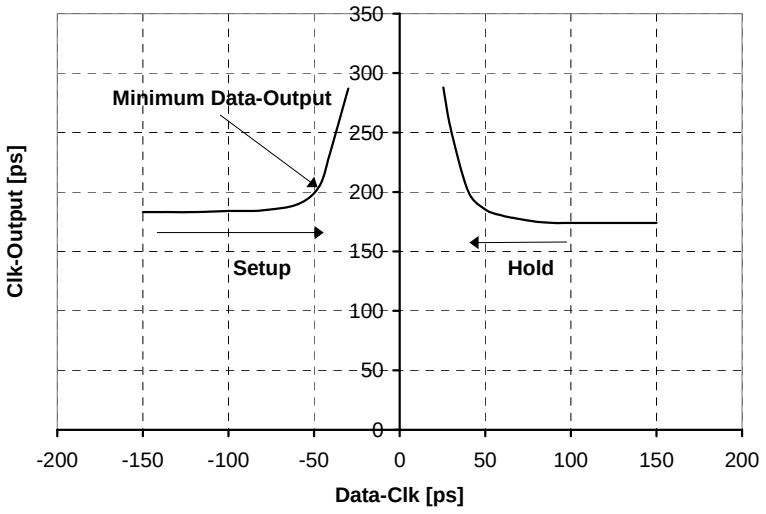


Setup time is a fairly vague concept

- The correct data can be captured but the delay can be greatly affected
- Where is the threshold?

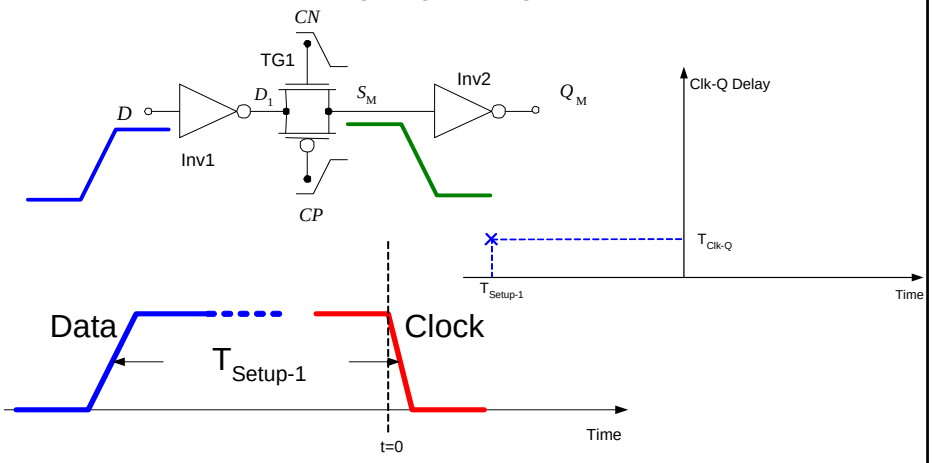
Minimum D-Q delay is the fastest possible way to transfer input to output, related to the sum of T_{setup} and T_{clk-Q}

CLK-Q vs. Setup/Hold Times



Setup Time Illustrations

Circuit before clock arrival (Setup-1 case)



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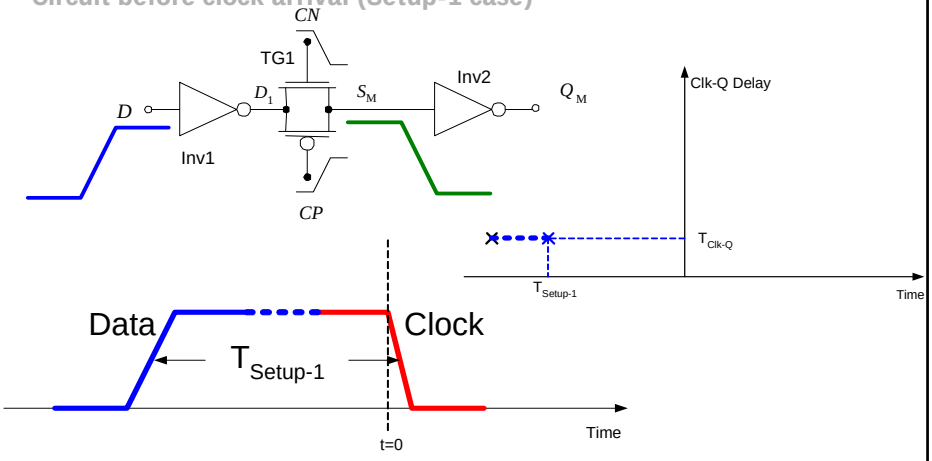

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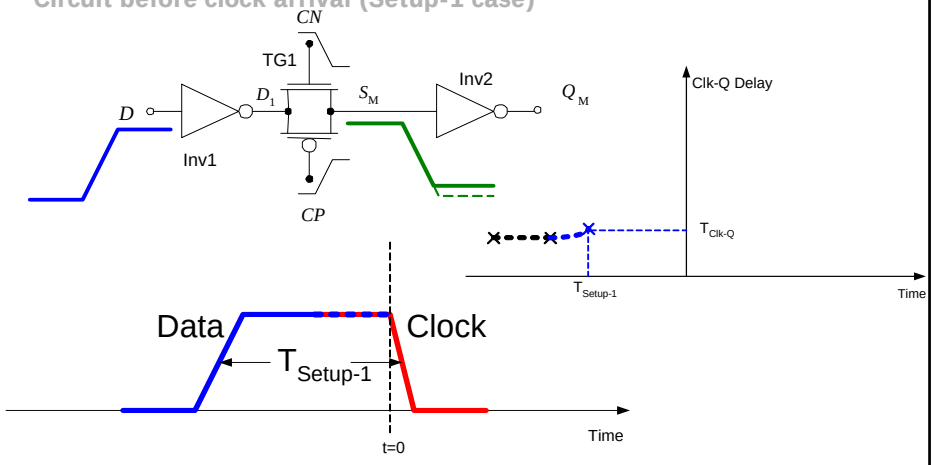

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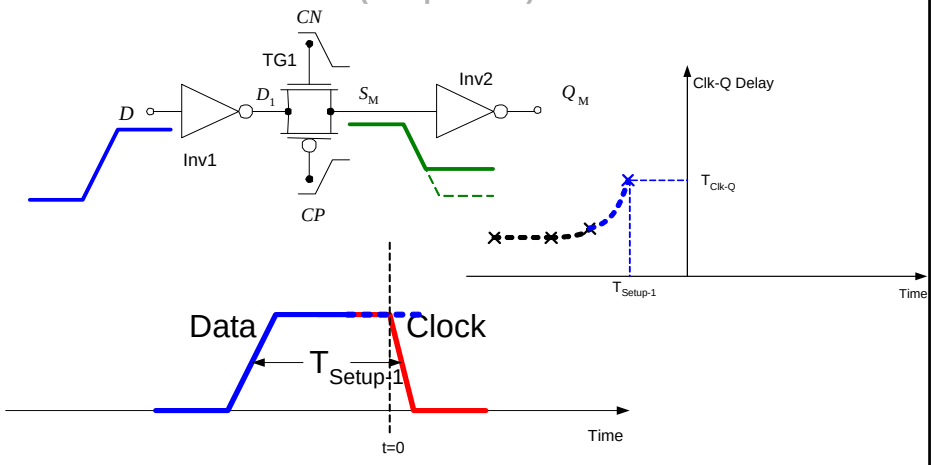

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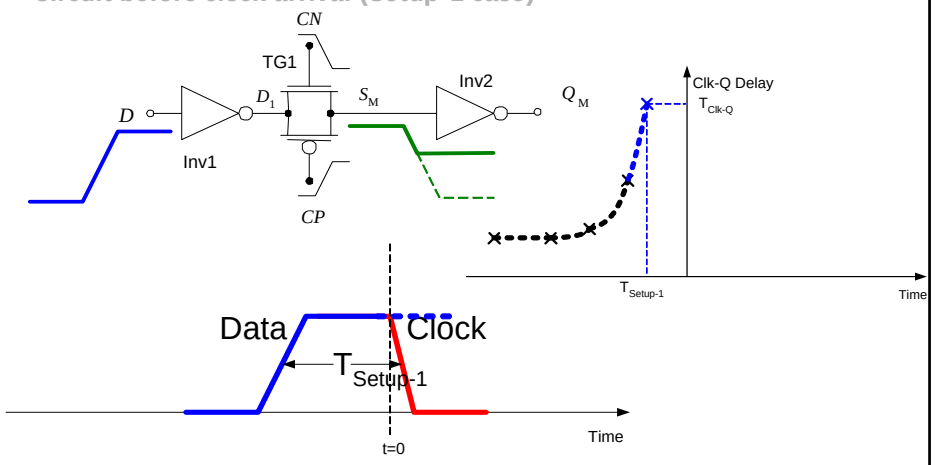


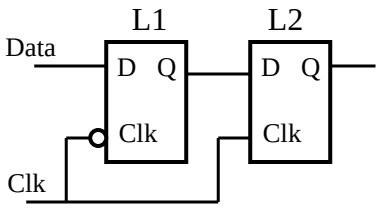
D-Q and setup time summary

- Define setup time as the point at which CLK-Q delay rises 5% beyond nominal
  - Nominal is measured when data arrives much earlier than CLK edge
  - This corresponds roughly to where the total D-Q delay is minimized

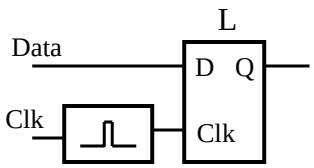
Pulse-Triggered Registers
An Alternative Approach

Ways to design an edge-triggered sequential cell:

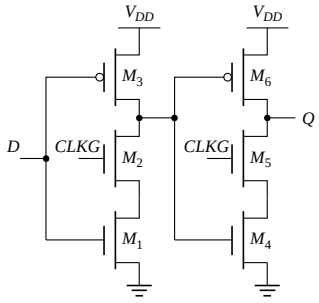
Master-Slave Latches



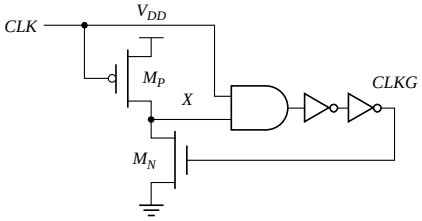
Pulse-Triggered Latch



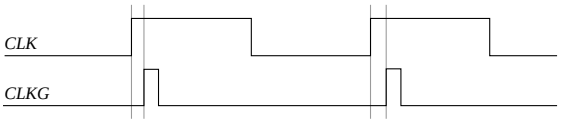
Pulsed Register



(a) register



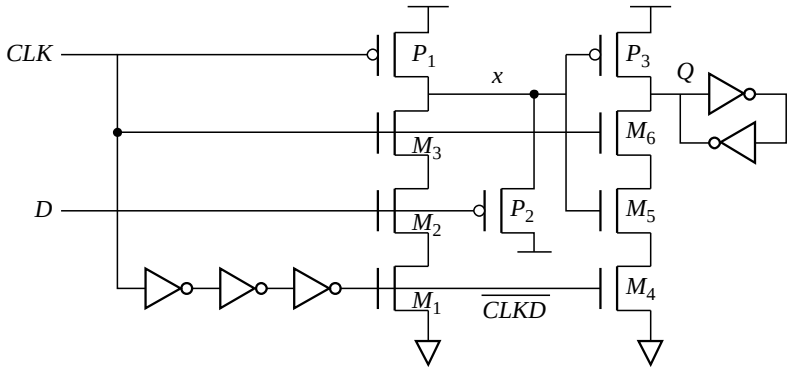
(b) glitch generation



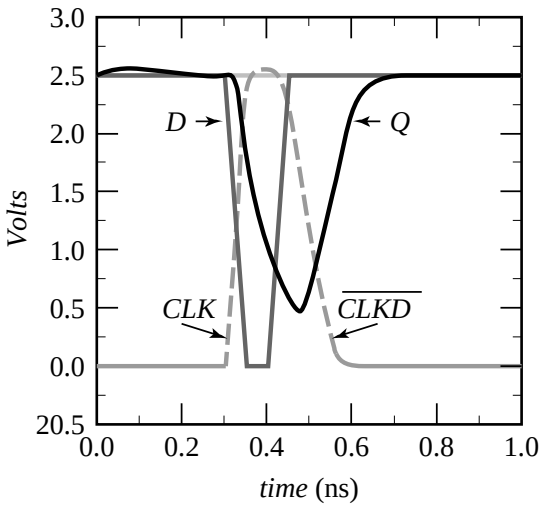
(c) glitch clock

Another Pulsed Register Topology

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7:

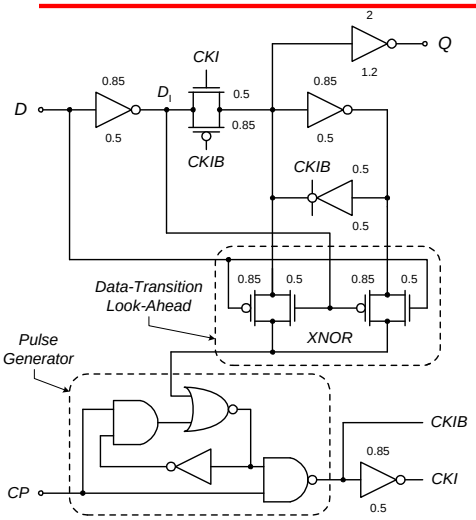


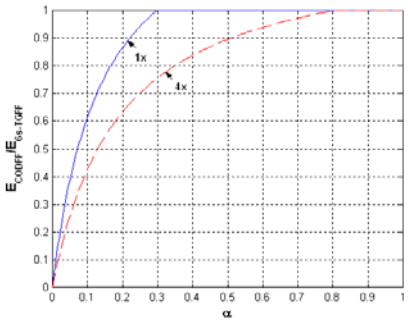
Pulsed Register Timing Diagram



- Negative setup times
- Fast CLK-Q delays
- Limited transparency window (similar to master-slave topology)
- Large hold times

Local Clock Gating





'Clock on demand' Flip-flop

Summary

- Sequential elements eat up a significant amount of total timing budget + power resources
  - Extremely important to design carefully
  - Robustness is also critical
- D-Q delay is best overall performance measure for edge-triggered registers since it combines both setup and CLK-Q delays
- New designs like pulsed registers provide enhanced performance with added design complexity