EECS 427
Lecture 23/24: Power grid issues

Last Time

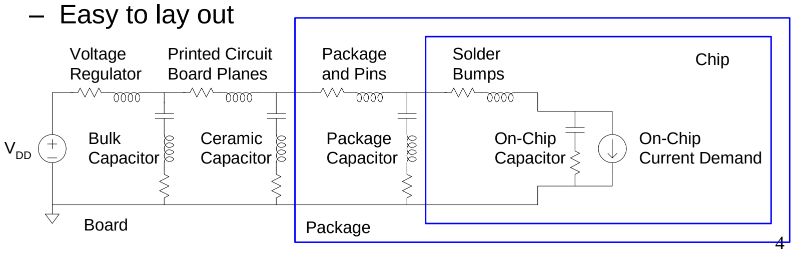
- Circuit techniques to reduce delay and power in global buses
  - – Reducing voltage swing through Vth drops
  - – Pulsed static buses avoid worst-case switching behavior + exploit monotonic switching

Lecture Overview

- Power grid issues
  - Noise and impact
  - Thermal issues
- Exam 2 next Thursday

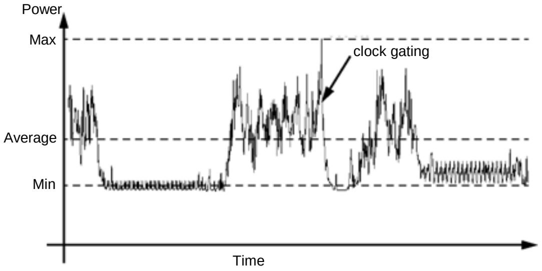
Power Distribution

- Power distribution network goals
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid electromigration & self-heating wearout
  - Consume little chip and wire area
  - Easy to lay out



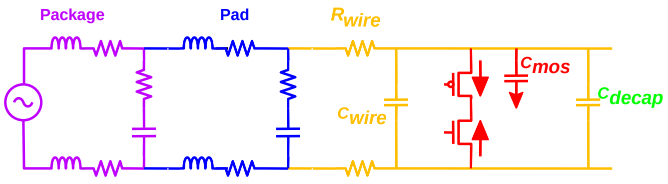
Stability Requirements

- $V_{DD} = V_{DDnominal} - V_{droop}$
- Want $V_{droop} < \pm 10\%$ of V_{DD}
- Sources of V_{droop}
  - IR drop
  - L di/dt noise
- I_{DD} changes on many time scales



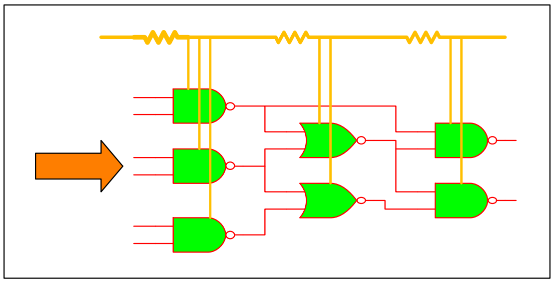
IR-Drop Problem

- Current supplied from voltage source to switching devices traverses a non-ideal power network. This causes the supply voltage appearing at the switching devices to deviate from ideal voltages



IR-Drop Problem

- In response to inputs, gates switch drawing current from the power rails
- As current is drawn, the voltage supplied to gates deviates from ideal supply voltage



Technology Trends

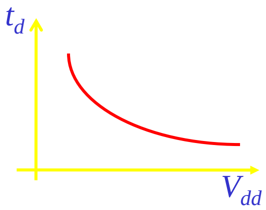
- Power consumption of chips increasing while power supply voltages are being reduced
  - greater current demands and larger drops
- Chips have become larger
  - implies longer power lines and hence larger drops
- Impact of IR-drops on performance and signal integrity is stronger
  - IR-drops can become a larger percentage of rail-to-rail voltages

Analysis and correction of IR-drop integrity is critical

Power distribution networks will take up more of the metallization (and design) resources

Impact: Performance

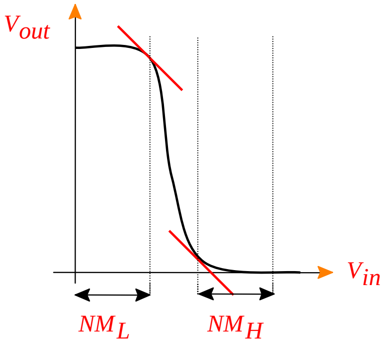
- Reduction in rail-to-rail voltage degrades performance
  - Current drive
  - Propagation delay



- Cell characterization and custom circuit design done with pre-defined budgets for IR-drop
  - drops larger than the budget causes performance problems

Impact: Reduced Noise Margins

- Noise margin reduces as rail-to-rail voltage swing reduces
  - Circuits become more susceptible to false switching due to noise



Correcting IR-Drop Problems

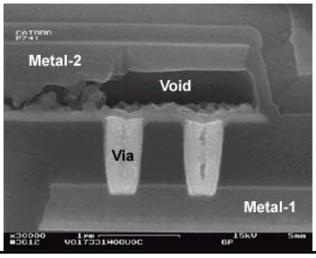
- Large drop at a particular location
  - Widen existing wires
  - Add new wires
- Add more power pads

Related Effect: Electromigration

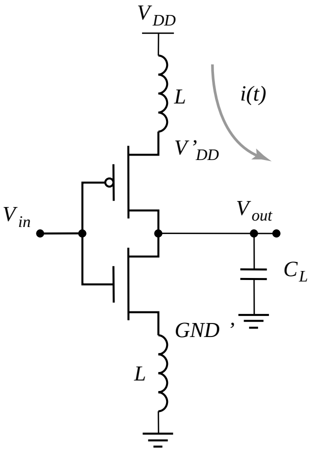
- Electromigration is the gradual wear of metal wires due to migration of metal atoms
  - protrusions and holes can cause opens or shorts
  - increased resistance causing higher voltage drops
- EM is directly proportional to DC current density
- High current density in Vdd and Gnd wires causes electromigration problems
  - power lines are more vulnerable than signal lines because of unidirectional current

Electromigration

- Vias are especially susceptible to electromigration problems
  - Typically a bottleneck in terms of cross-sectional area through which current can flow
  - Use via arrays
  - Current crowding stresses vias unequally
    - Current crowds around edges of vias rather than using the entire cross-sectional area



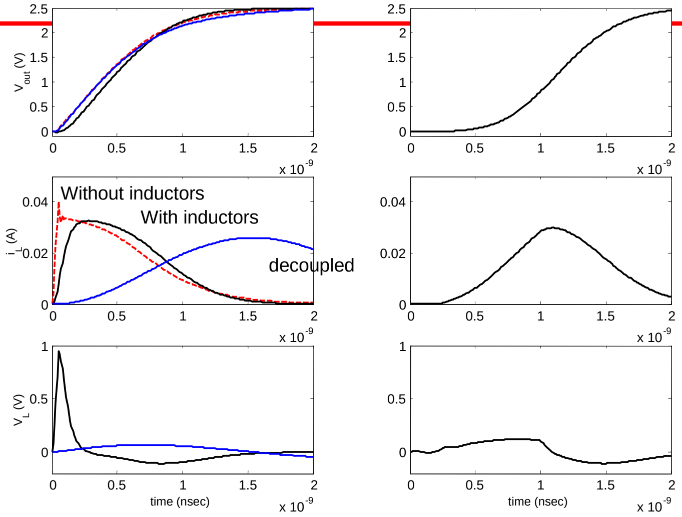
L di/dt



Impact of inductance on supply voltages:

- Change in current induces a change in voltage
- Longer supply lines and cheaper packages have larger *L*

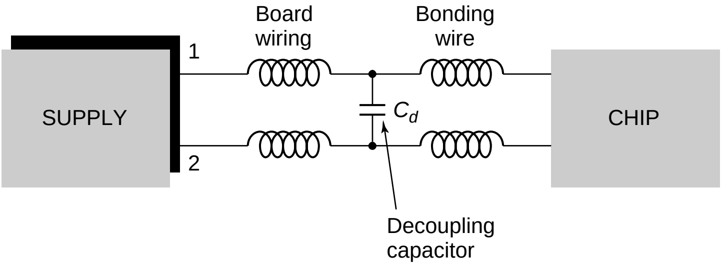
L di/dt: Simulation



Input rise/fall time: 50 psec

Input rise/fall time: 800 psec

Decoupling Capacitors



Decoupling capacitors are added:
- on the board (right under the supply pins)
- on the chip (under the supply straps, near large buffers)

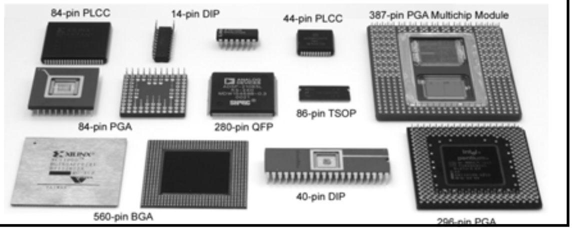
They help by acting as a local power supply (charge reservoir) for high frequency current draw

Dealing with Ldi/dt

- Separate power pins for I/O pads and chip core
- Multiple power and ground pins
- Increase rise and fall times of off-chip signals to maximum extent allowable
- Use advanced packaging technologies
- Add decoupling capacitances
  - Typically use MOSFETs with source/drain shorted, large capacitance per unit area due to thin gate oxide

Heat Dissipation

- 60 W light bulb has surface area of 120 cm^2
- Itanium 2 die dissipates 130 W over 4 cm^2
  - Chips have enormous power densities
  - Cooling is a serious challenge
- Package spreads heat to larger surface area
  - Heat sinks may increase surface area further
  - Fans increase airflow rate over surface area
  - Liquid cooling used in extreme cases ($$$)

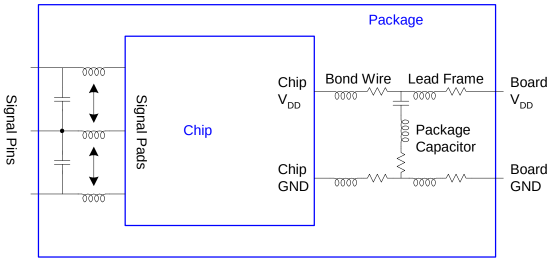


Thermal Resistance

$\Delta T = \theta_{ja}P$

- ΔT: temperature rise on chip
- θ_{ja}: thermal resistance of chip junction to ambient
- P: power dissipation on chip

- Thermal resistances combine like resistors
  - Series and parallel
- $\theta_{ja} = \theta_{jp} + \theta_{pa}$
  - Series combination



Example

- Your chip has a heat sink with a thermal resistance to the package of 4.0° C/W
- The resistance from chip to package is 1° C/W
- The system box ambient temperature may reach 55° C
- The chip temperature must not exceed 100° C
- What is the maximum chip power dissipation?

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- (100-55 C) / (4 + 1 C/W) = 9 W

Summary

- Power grid stability is difficult to achieve due to rising power budget and lower voltages (much higher currents in the supply grid)
  - IR drop can be limited through proper grid sizing
  - L*di/dt is a tougher problem; slow things down + add lots of capacitance between Vdd/GND