EECS 427
Lecture 3: Design Styles Overview

Reading: 8.1 - 8.4

Last Time

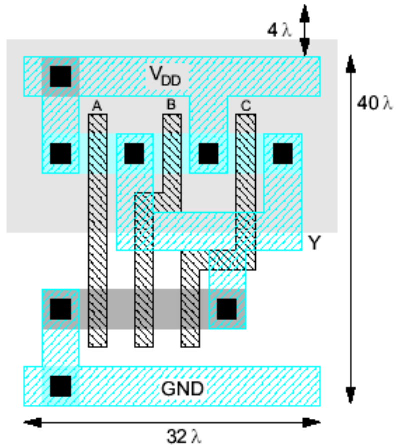
- Finished processing/fabrication discussion
  - Important to be able to visualize what your layout translates to in silicon
  - We use a 0.13um twin-well process
    - But min channel length is 0.12um, p well is implied
- Design rules are guidelines that ensure adequate yield of final design
  - Designers want small/compact, process engineers want larger & easier to print
  - Compromise

Outline

- Design styles
  - Custom
  - Semi-custom or ASIC (standard cells)

Example Layout: NAND3

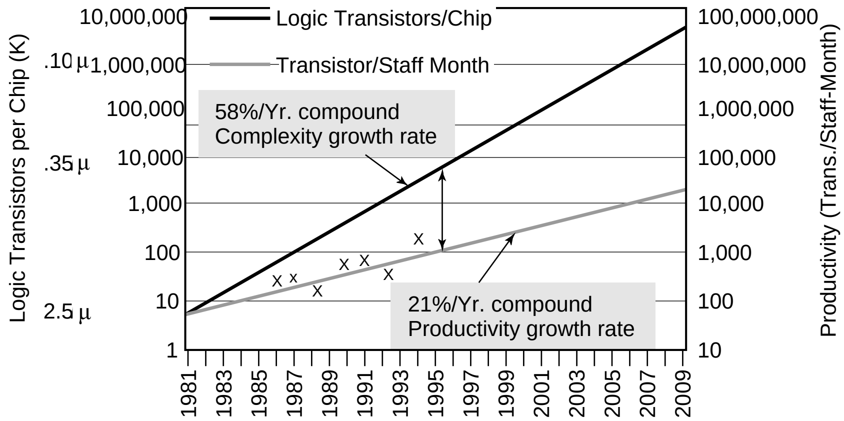
- Horizontal n-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ



Design Styles: Key points

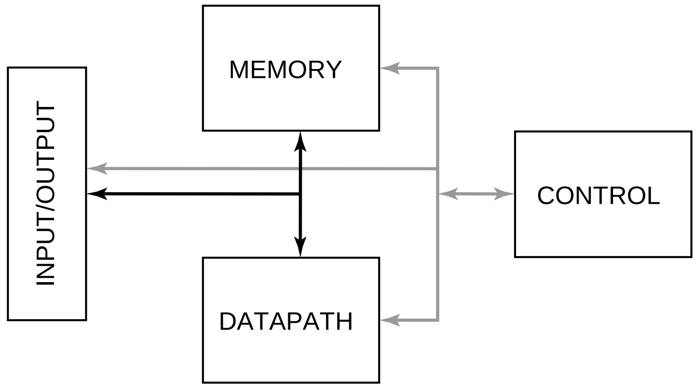
- Hierarchy must be used to design at the current levels of complexity
- Design teams in industry: focus on a specific sub-system like the adder or register file, etc.
  - In 427, we want you to gain experience with ALL these components
- Custom == high performance, lowest power
  - Humans design better circuits than software
    - But at a **much** slower rate
- Automated == faster design times
  - Often with 6-8X worse overall performance

The Design Productivity Challenge

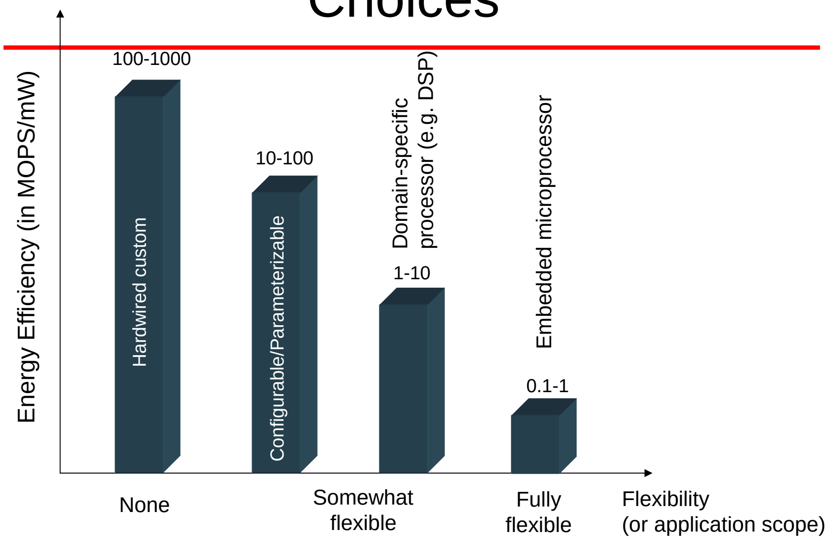


A growing gap between design complexity and design productivity

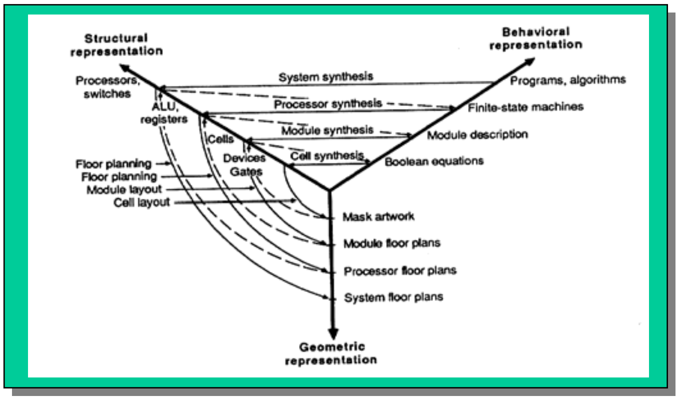
A Simple Processor



Impact of Implementation Choices

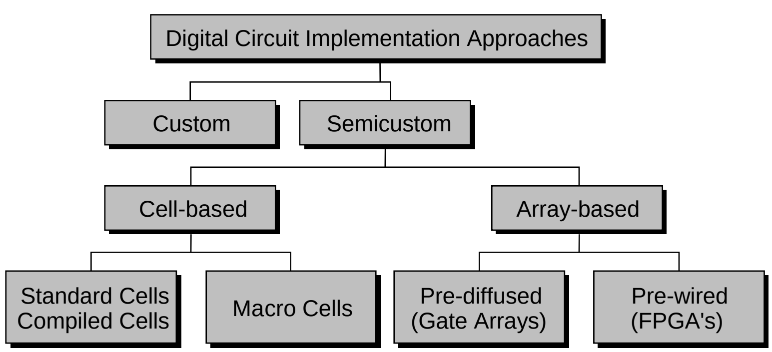


Design Methodology

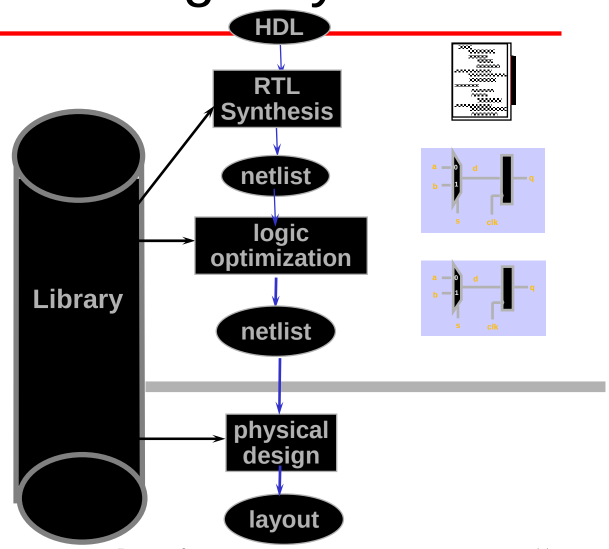


• Design process traverses iteratively between three levels of abstractions: behavior, structure, and geometry
• More and more automation for each of these steps

Implementation Choices

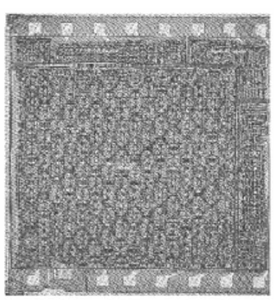


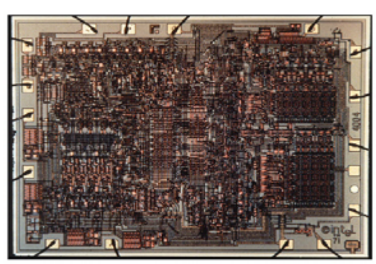
ASIC design style



The Custom Approach

- 1970's processes usually had only NMOS transistors
  - Inexpensive, but consume power while idle

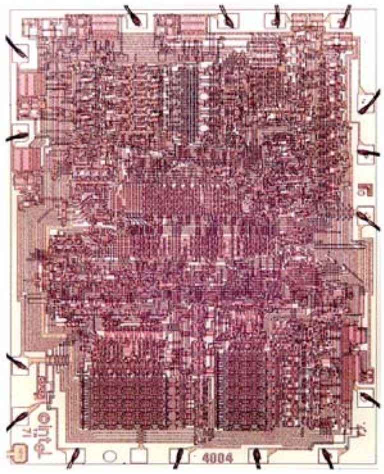




Intel 1101 256-bit SRAM Intel 4004 4-bit μProc

- 1980s-present: CMOS processes for low static power

The Custom Approach

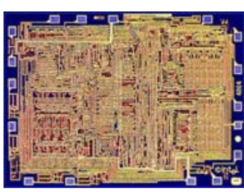


Intel 4004
First microprocessor
1971

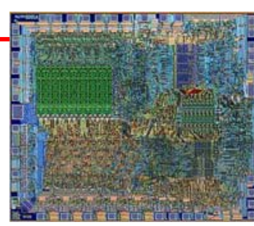
www.intel4004.com

Courtesy Intel

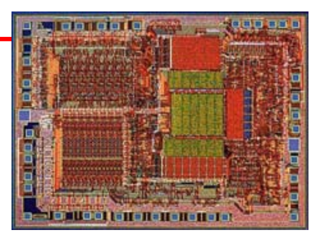
Transition to Automation and Regular Structures



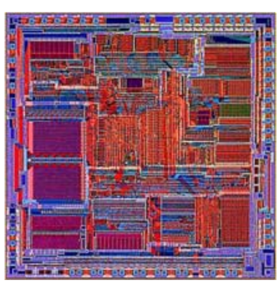
Intel 4004 ('71)



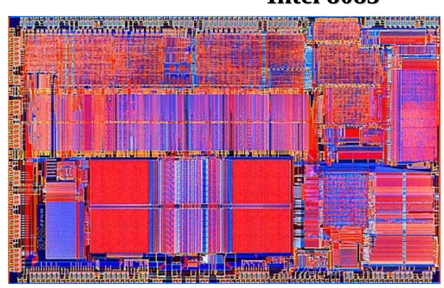
Intel 8080



Intel 8085



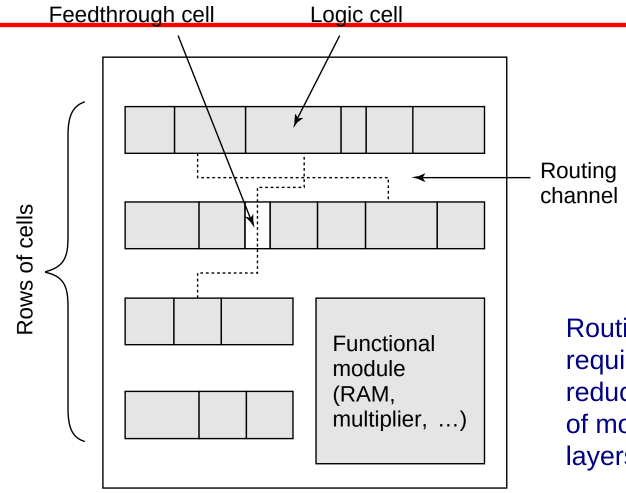
Intel 8286



Intel 8486

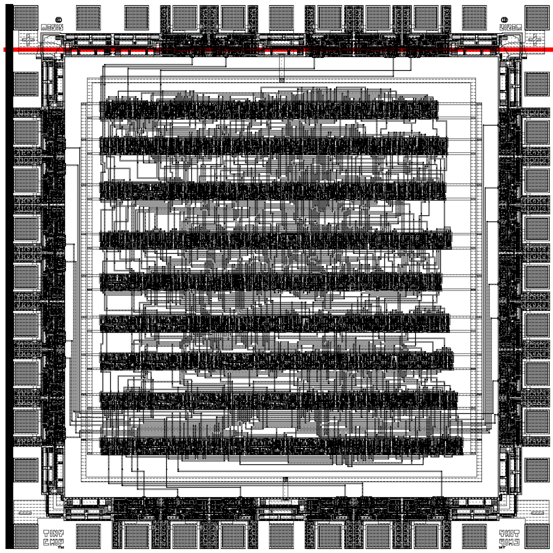
Courtesy Intel

Cell-based Design (or standard cells)



Routing channel requirements are reduced by presence of more interconnect layers

Standard Cell — Old Example



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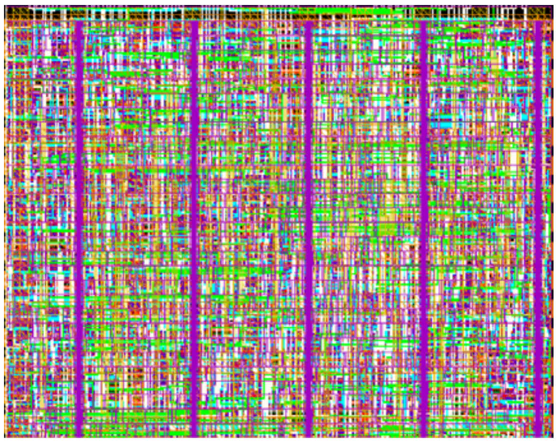
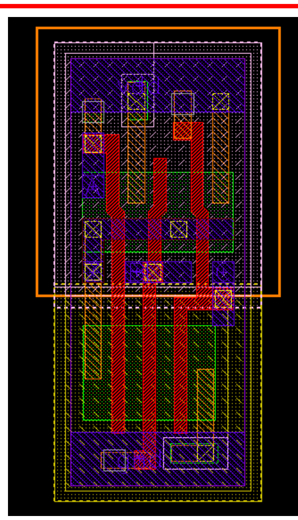
Standard Cell – The New Generation



Cell-structure hidden under interconnect layers

<u>Over the cell</u> routing

Standard Cell - Example



Path	1.2V - 125°C	1.6V - 40°C
$In1—t_{pLH}$	$0.073+7.98C+0.317T$	$0.020+2.73C+0.253T$
$In1—t_{pHL}$	$0.069+8.43C+0.364T$	$0.018+2.14C+0.292T$
$In2—t_{pLH}$	$0.101+7.97C+0.318T$	$0.026+2.38C+0.255T$
$In2—t_{pHL}$	$0.097+8.42C+0.325T$	$0.023+2.14C+0.269T$
$In3—t_{pLH}$	$0.120+8.00C+0.318T$	$0.031+2.37C+0.258T$
$In3—t_{pHL}$	$0.110+8.41C+0.280T$	$0.027+2.15C+0.223T$

3-input NAND cell
(from ST Microelectronics):
C = Load capacitance
T = input rise/fall time

Typical Standard Cell Library

Gate Type	Variations	Options
Inverter / buffer / tristate buffers		Wide range of power options, 1X, 2X, 4X, 8X, 16X, 32X, 64X minimum size inverter
NAND / AND	2–8 inputs	High, normal, low power
NOR / OR	2–8 inputs	High, normal, low power
XOR / XNOR		High, normal, low power
AOI / OAI		High, normal, low power
Multiplexers	Inverting/noninverting	High, normal, low power
Schmitt trigger		High, normal, low power
Adder / half adder		High, normal, low power
Latches		High, normal, low power
Flip-flops	D, with and without synch/asych set and reset, scan	High, normal, low power
I/O pads	Input, output, tristate, bidirectional, boundary scan, slew rate limited, crystal oscillator	Various drive levels (1–16 mA) and logic levels

Relative performance, custom vs. ASIC design methodologies

Factor	vs. Poor ASIC	vs. Best Practice ASIC
Microarchitecture (e.g., pipelining)	1.8x	1.3x
Sequencing overhead: elements, skew, time borrowing	1.45x	1.1x
Circuit families (e.g., domino)	1.4x	1.2x
Logic design	1.3x	1.0x
Cell design, cell sizing, and wire sizing	1.45x	1.1x
Layout: floorplanning, placement, wire management	1.4x	1.0x
Exploiting process variation and accessibility	2x	1.2x

Summary

- Semicustom (or ASIC, standard cell based) vs. Custom is an old debate
  – Entire book on “Closing the gap between custom and ASIC”
  – Key is how to achieve custom-like performance with ASIC-like design times
- Standard cell libraries are pre-characterized and are the best example of *design reuse*
  – Libraries are getting richer and richer → semicustom becomes a fitting description