EECS 427
Lecture 4: CMOS review & Dynamic Logic

Reading: 5.4, 5.5, 6.2, 6.3

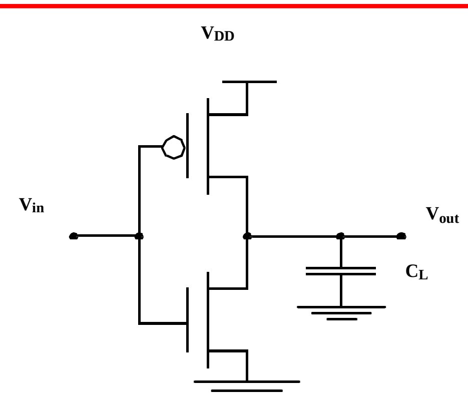
Overview

- CMOS basics
- Power and energy in CMOS
- Dynamic logic
- CAD2 available online
- HW1 turned in Friday
- HW2 due in 1 week
  - Email dennis@eecs.umich.edu, 1 email per group, include background of each person in ckts, architecture, or devices
  - Choose teams of 4 (we may need a couple teams of 5)
  - Mix of EE and CE backgrounds ideal

CMOS Properties

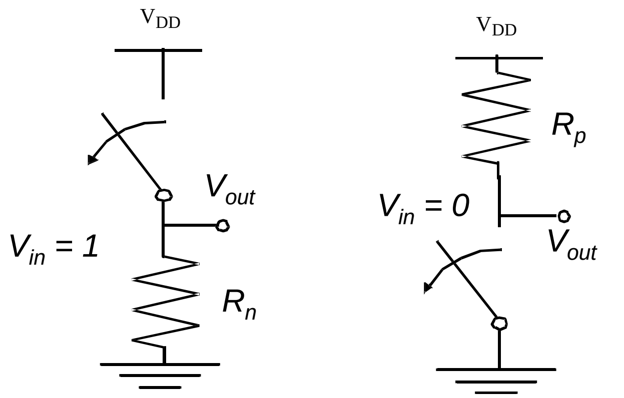
- Full rail-to-rail swing; high noise margins
- Logic levels not dependent upon the relative device sizes; ratioless
- Always a path to Vdd or Gnd in steady state; low output impedance
- Extremely high input resistance; nearly zero steady-state input current
- No direct path steady state between power and ground; no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors

The CMOS Inverter



First DC analysis, then transient analysis

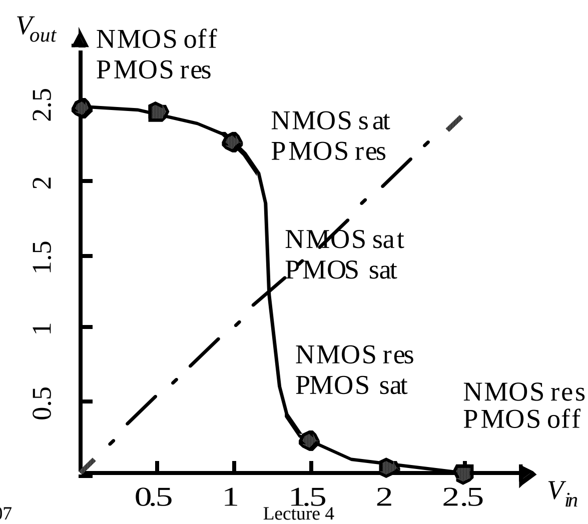
CMOS Inverter
First-Order DC Analysis



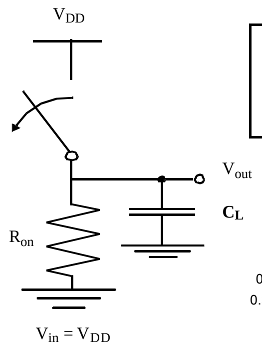
$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

CMOS Inverter VTC

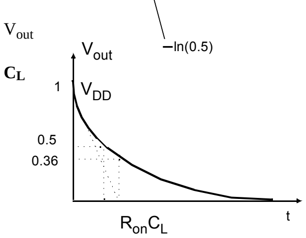
Noise margins



CMOS Inverter: First Order Transient Response



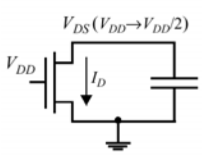
$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$



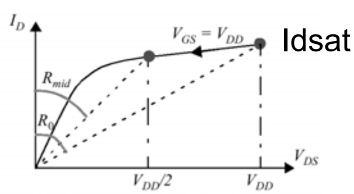
How do is R_{on} calculated?

CMOS Performance Analysis

Propagation delay: $t_{pHL} = 0.69 R_{eqn} C_L$ $t_{pLH} = 0.69 R_{eqp} C_L$



(a) schematic



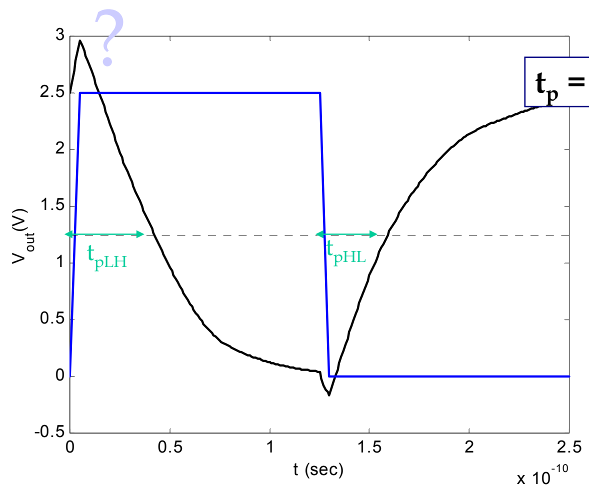
(b) trajectory traversed on ID-VDS curve.

Average the large signal resistance at endpoints of voltage transition of concern (0-50%)

At 0% → V/I is Vdd/Idsat

At 50% → V/I is (Vdd/2)/(a*Idsat) where a < 1

Transient Response



$t_p = 0.69\ C_L\ (R_{eqn}+R_{eqp})/2$

If a≈0.9, then
Req=0.8*Vdd/Idsat

MOS Capacitances

1) Gate to channel cap
2) Drain to bulk and source to bulk (junction) cap
3) Overlap cap, C_{gd0} and C_{gs0}

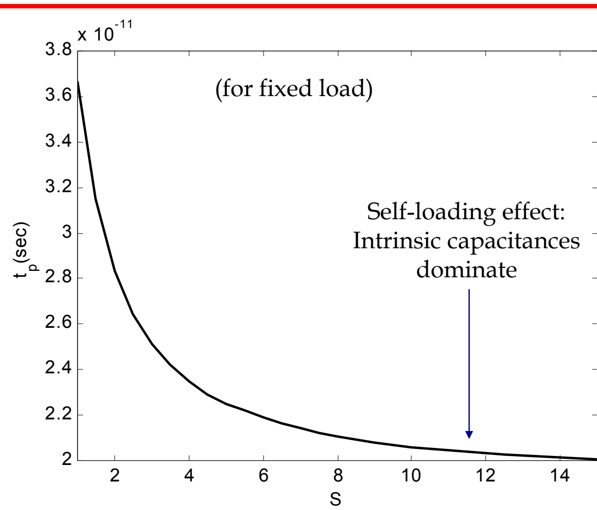
Capacitance parameters for book's 0.25µm process

	C_{ox} (fF/µm²)	C_O (fF/µm)	C_j (fF/µm²)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

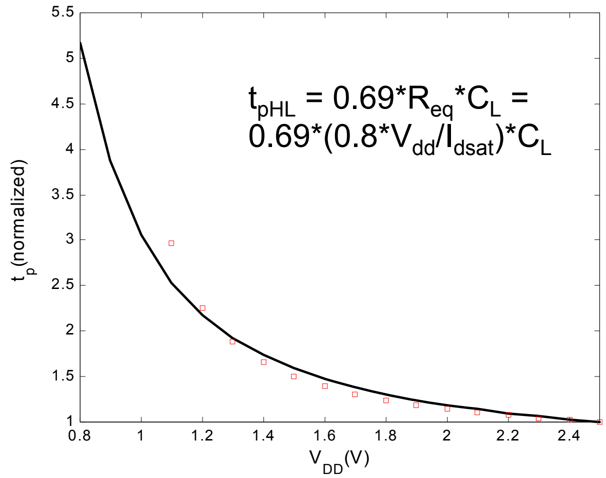
Design for Speed

- Keep capacitances small
  - Compact layout, good placement (short wires)
- Increase transistor sizes to match load
  - watch out for self-loading!
- Increase V_{DD}
  - Not usually possible due to reliability and power penalties

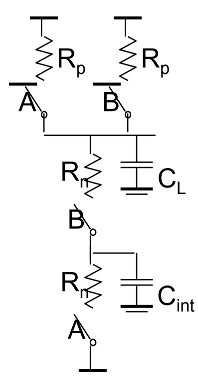
Device Sizing



Delay as a function of V_{DD}



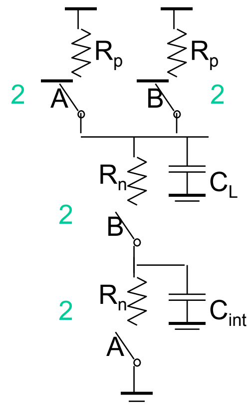
Input Pattern Effects on Delay

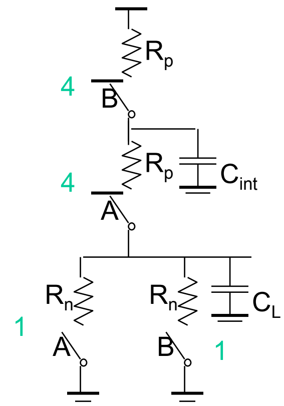


2-input NAND

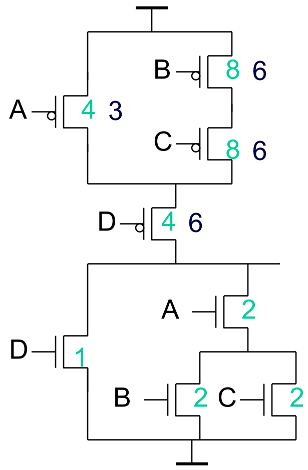
- Delay is dependent on the pattern of inputs
- Low to high transition
  - both inputs go low
    - delay is $0.69\ R_p/2\ C_L$
  - one input goes low
    - delay is $0.69\ R_p\ C_L$
- High to low transition
  - both inputs go high
    - delay is $0.69\ 2R_n\ C_L$

Transistor Sizing





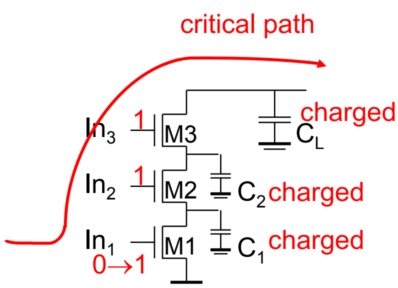
Sizing a Complex CMOS Gate



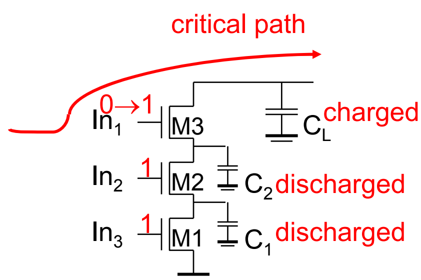
$OUT = \overline{D + A \cdot (B + C)}$

Fast Complex Gates: Design Techniques

- Transistor ordering



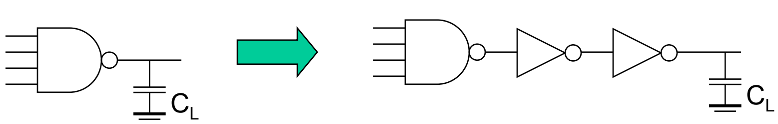
delay determined by time to discharge C_L, C_1 and C_2



delay determined by time to discharge C_L

Fast Complex Gates: Design Techniques

- Isolating fan-in from fan-out using buffer insertion



Summary of CMOS Basics

- CMOS is the dominant circuit family due to:
  - No static power consumption (more next time on this)
  - Ease of design
  - Robust to variations and noise

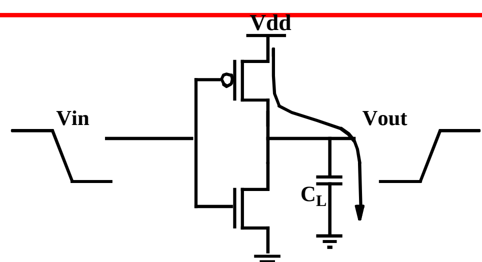
Power and Energy Figures of Merit

- Power consumption in Watts
  - determines battery life in hours
  - Ex: Laptop battery rated at 65 W-hr
- Peak power
  - determines power and ground wiring requirements
  - sets packaging limits (plastic vs. ceramic)
- Energy in units of Joules
- Energy = power * time
  - Joules = Watts * seconds
  - lower energy means less power to perform a computation at the same frequency

Where Does Power Go in CMOS?

- Dynamic power consumption
  - Charging and discharging of capacitors
- Short-circuit currents
  - During switching transients, current flows between Vdd and GND
  - Not dominant – typically assumed to be ~10% of dynamic power
- Static power consumption
  - Leakage: due to non-ideal switches

Dynamic Power Consumption



Energy per transition:

$$E_{Vdd} = \int_0^{\infty} i_{vdd}(t)\, V_{dd}\, dt = V_{dd} \int_0^{\infty} C_L \frac{dv_{out}}{dt} dt = C_L V_{dd} \int_0^{V_{dd}} dv_{out} = C_L V_{dd}^2$$

The book claims that power/energy is independent of device sizing → misleading since device sizes primarily determine C_L

Can reduce C_L, V_{dd}, and *f* to minimize power

Energy vs. Power

Each transition on C_L requires $C_L * V_{dd}^2$ of energy BUT 1/2 of this energy is lost (to heat) while the other half is *stored* (or *removed)* on/from the capacitor

For every transition, $C * V_{dd}^2/2$ of energy is **consumed**

For every period (both a L→H and H→L transition on C_L), $C * V_{dd}^2$ of energy is consumed

Then, power = rate of energy consumption so:

$P_{dyn} = C_L * V_{dd}^2 * f_{sw}$

Where f_{sw} is the frequency with which C_L switches

Switching Activity, α_{sw}

Let $f_{sw} = \alpha_{sw} * f_{clock}$ since we usually know clock frequency of a design (e.g. 3 GHz Core 2 Duo)

$$\mathbf{0 < \alpha_{sw} < 1}$$

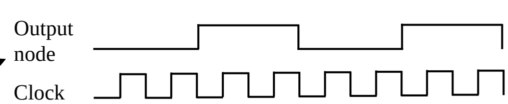
For $\alpha_{sw} = 0$, the circuit never switches so no dynamic power is consumed

For $\alpha_{sw} = 1$, the node switches as often as the clock (the circuit cannot switch more often than this) so $f_{sw} = f_{clock}$

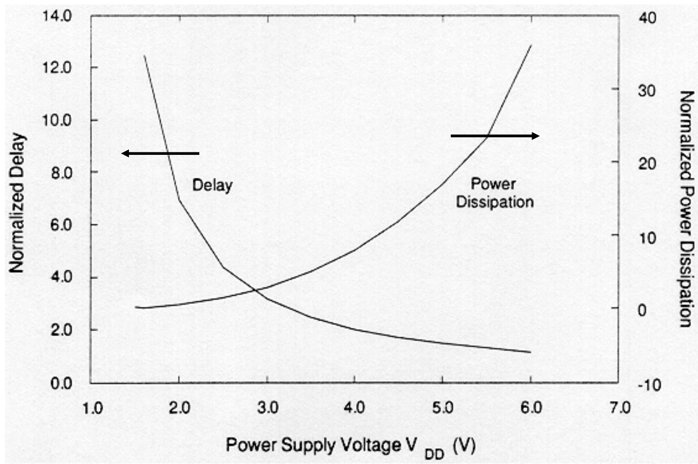
Most cases → somewhere in between

Lower α_{sw} = lower power

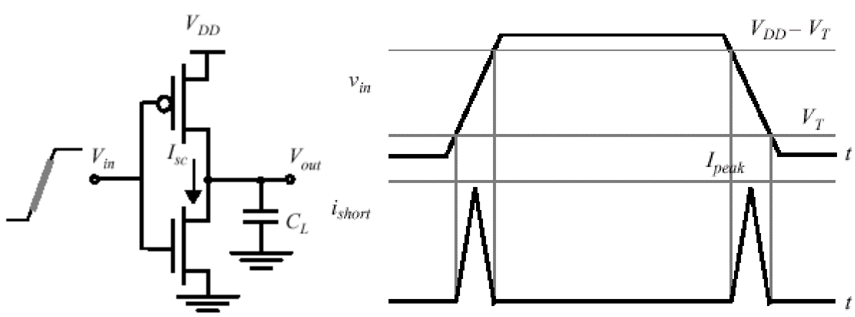
$\alpha_{sw} = 0.25$



Fundamental Tradeoff: Power vs. Delay



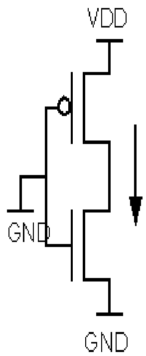
Short-circuit Power



During input switching, both NMOS and PMOS are ON for a small amount of a time

Some current is “lost” – meaning it’s not used to charge/discharge the capacitor, but flows to the other supply rail

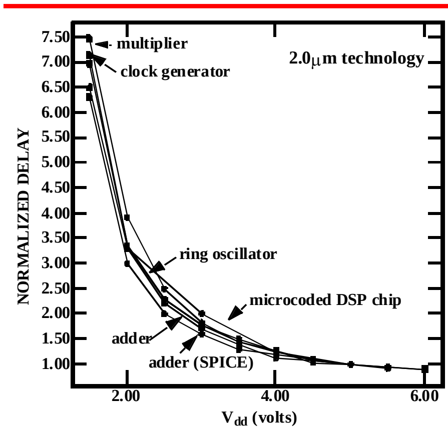
Static Power Consumption



- not completely OFF
- $P_{static} = V_{DD} \cdot I_{off}$
- static dissipation becomes important in CMOS

Wasted energy …
Should be avoided as much as possible

Lower V_{dd} Increases Delay



$$T_d = \frac{C_L * V_{dd}}{I}$$

$$I \sim (V_{dd} - V_t)^2$$

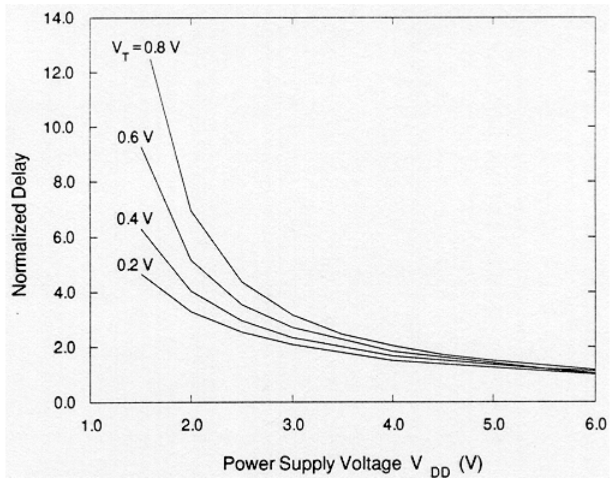
$$\frac{T_{d(Vdd=2)}}{T_{d(Vdd=5)}} = \frac{(2) * (5 - 0.7)^2}{(5) * (2 - 0.7)^2}$$

$$\approx 4$$

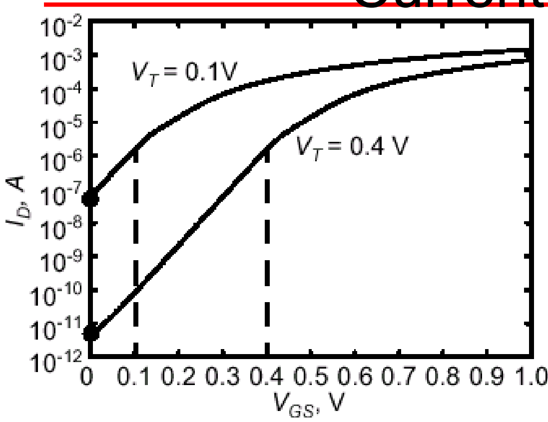
The exponent will change next time we see this…

- **Relatively independent of logic function and style.**

Reducing V_{th} to offset delay penalty



Subthreshold Leakage Current



Subthreshold swing (Ss) is inverse of slope in subthreshold (cut-off) region

Remains constant when V_{th} is shifted

Note log scale on y-axis

Off-current defined as how much current a device conducts when V_{gs} = 0V [and V_{ds} = V_{dd}]

Example Calculation

$I_{off} \sim 10\mu A/\mu m * 10^{-Vth/Ss}$

Subthreshold swing (S_s) is around 80-100 mV/decade

Let V_{th} be 0.3V and S_s = 100 mV/dec

I_{off} = 10 nA/µm

Assume 10^7 inverters in a design (not a good design…) with W_n = 1µm

Total $I_{off} = 10^7 * 10nA = 100mA$
P_{static} = 2V*100mA = 0.2W

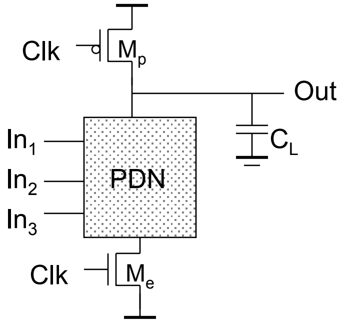
Summary of Power in CMOS

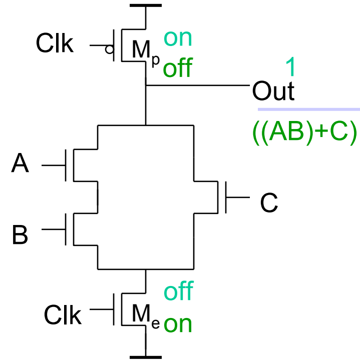
- Power reduction is as important as increasing speed in IC design today (design techniques to be described later in semester)
- Three major components of power in CMOS
  - Dynamic: charging capacitors → dominant
  - Short-circuit: small, typically ignore
  - Static: subthreshold leakage, growing fast

Dynamic CMOS

- In **static** circuits in steady-state (i.e., when not actively switching) the output is connected to either GND or V_{DD} via a low resistance path
- **Dynamic** circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes
  - Caps are left floating at times; noise sensitive

Dynamic Gate





Two phase operation
Precharge (Clk = 0)
Evaluate (Clk = 1)

Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation
- Inputs to the gate can make at most one transition during evaluation phase

- Output can be in the high impedance state during evaluation (PDN off), state is stored on C_L

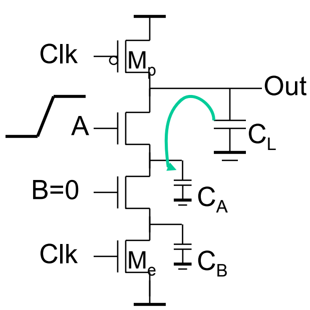
Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  – number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds (1.5-2X vs. static CMOS)
  – reduced load capacitance due to **lower input** capacitance (C_{in})
  – reduced load capacitance due to smaller output loading (Cout)
  – NMOS only, faster devices (optimize for one transition direction)
  – no I_{sc}, so all the current provided by PDN goes into discharging C_L

Properties of Dynamic Gates

- Overall power dissipation **higher** than static CMOS
  - **higher transition probabilities** (most critical)
  - **extra load on Clk**
  - Smaller devices (caps) helps reduce impact
- PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}
  - Small low noise margin (NM_L)
- Need a precharge/evaluate clock

Issues in Dynamic Design: Charge Sharing

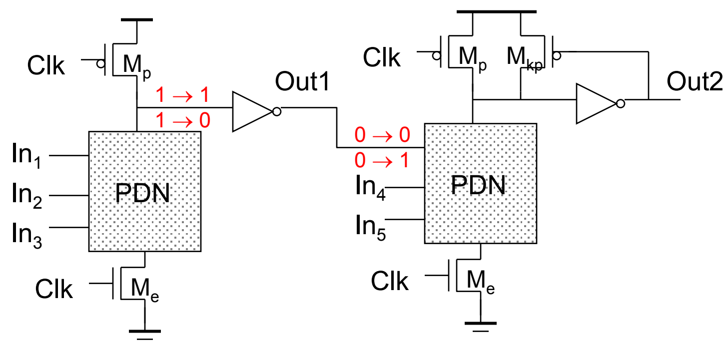


Charge stored originally on C_L can be redistributed (shared) over C_L and C_A leading to reduced robustness

To avoid:

1) Precharge internal nodes – adds delay
2) Add a feedback (keeper) device

Domino Logic

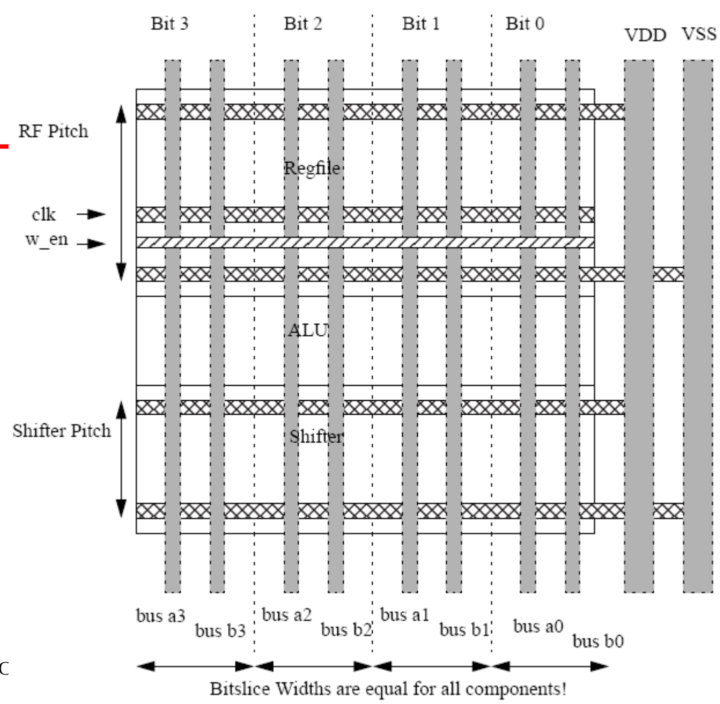


Summary of Dynamic Gates

- Dynamic gates provide speed benefits
- But:
  - – Add complexity
  - – Worsen power
  - – Worsen noise immunity

Bit Slice Width

- Bit slice width is layout width allocated to one bit of computation in datapath
- Controls aspect ratio of final design
- Establishes regularity
- Bit slice width matching avoids need for snaking data buses over the datapath
  - Pitch matching: cell heights in same functional unit should match to maintain continuity of power rails
    - Diff functional units can have diff cell heights
- Easier to visualize wiring tracks and estimate wire load



Effect of bit slice width

- A row of mux2 in the pipeline
- Large bit pitch → long select line (blue wire)
- Small bit pitch → long data line (red wire)

- 70-100 lambda formerly a rough guideline; equivalent to 4.2-6um width in your technology