EECS 427
Lecture 5: Interconnect review

Reading: 4.3.1, 4.3.2, 4.4.1-4.4.3, 9.3.3

Last Time

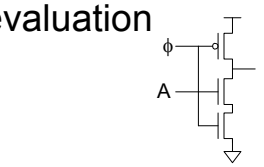
- Power/energy in CMOS
  - Sources we will focus on are dynamic (caps) and leakage (subthreshold currents)
  - Much more later in the class on low-power design techniques
- Dynamic logic
  - Used sparingly, when speed is critical
  - Increases power, design complexity, poor noise properties compared to CMOS
  - Revisit today

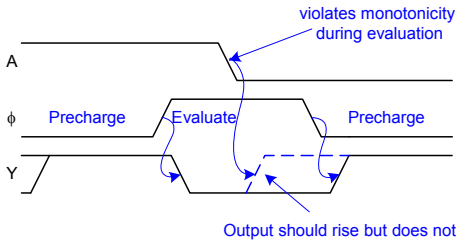
Overview

- Wiring or interconnections and their performance impact
  - Contribute to delay, RC
  - Coupling capacitance between wires
- Design strategies to deal with large RC or C delays
  - Repeaters and cascaded/tapered buffer chains

Monotonicity

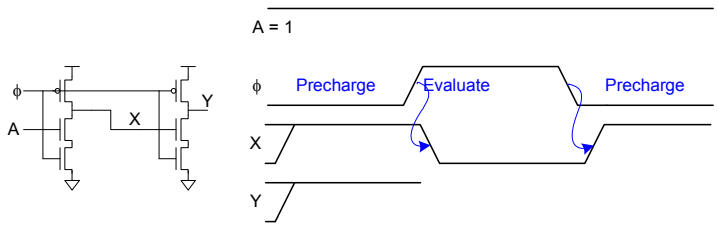
- Dynamic gates require *monotonically rising* inputs during evaluation
  - 0 -> 0
  - 0 -> 1
  - 1 -> 1
  - But not 1 -> 0





Monotonicity Woes

- But dynamic gates produce monotonically falling outputs during evaluation
- Illegal for one dynamic gate to drive another!



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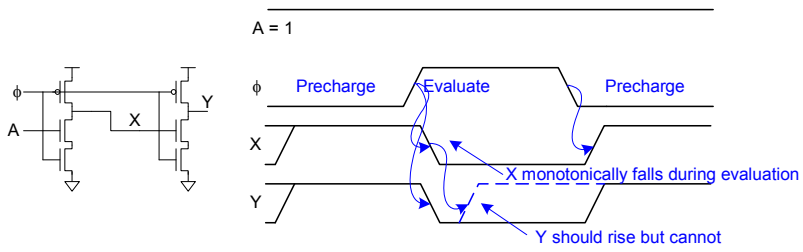
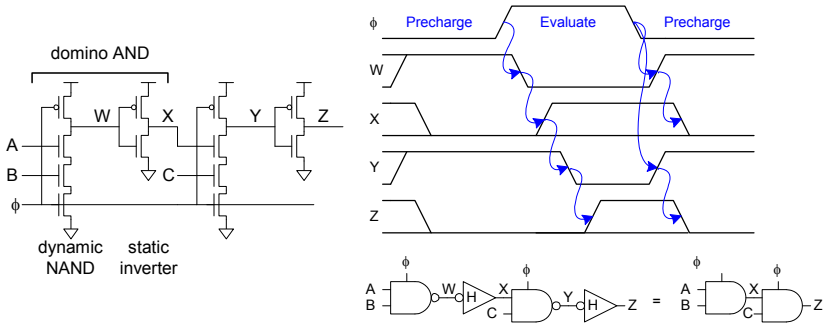


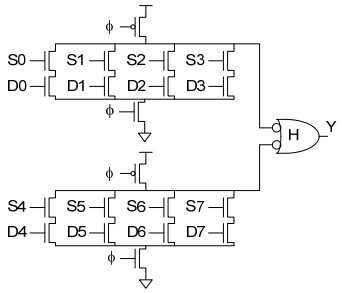
Domino Gates

- Follow dynamic stage with inverting static gate
  - Dynamic / static pair is called domino gate
  - Produces monotonic outputs

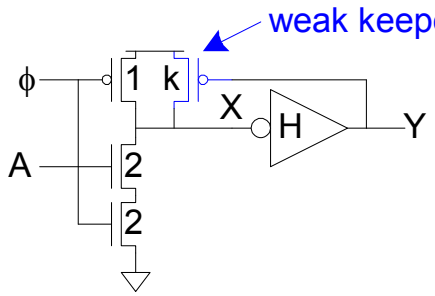


Domino Optimizations

- Each domino gate triggers next one, like a string of dominos toppling over
- Gates evaluate sequentially but precharge in parallel
- Thus evaluation is more critical than precharge
- Skewed static stages can perform added logic



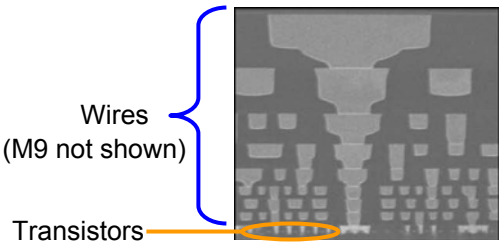
Keepers: A must-have



- Keeper helps with charge leakage, charge sharing
  - But – fights evaluation initially
- Must be kept very weak; often use L>Lmin and W=Wmin
- Avoid truly floating nodes!

Transistors vs. Wires

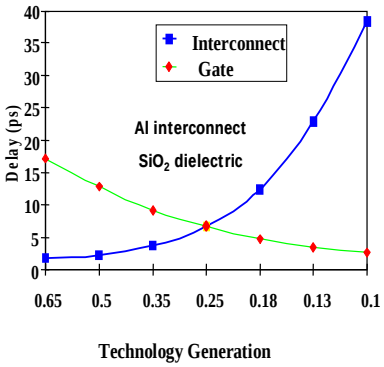
- Cross section of modern technology is mostly dominated by wires.



Cross section of
Intel 45nm technology
(IEDM 2007)

Reverse Scaling of Interconnects

- Gate delays reduce with technology scaling
- Global interconnect delays increase with scaling
  - Interconnects must be included in analysis and optimization



Interconnect Parasitics

- Classes of parasitics
  - Capacitance
  - Resistance
  - Inductance (627 focuses on this)
- Impact of interconnect parasitics
  - Increases propagation delay
  - Energy dissipation and power distribution
  - Reliability and signal integrity

Interconnect Modeling

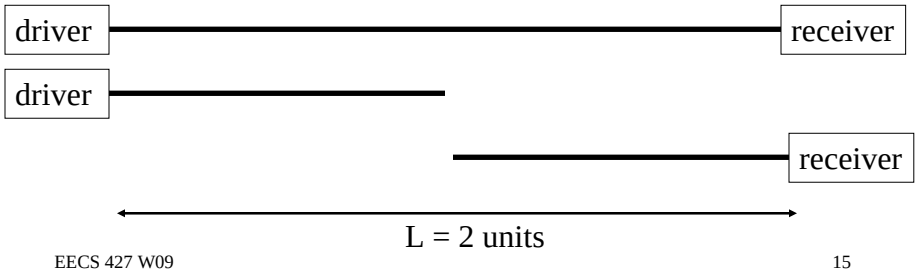
- Lumped capacitance model is what we use for device/gate analysis
- Lumped RC model
  - For simple one segment RC:
    - 50% Delay = 0.69*RC
    - 10-90% Slew = 2.2*RC
- Distributed RC line model
  - More accurate for interconnect analysis
    - 50% Delay = 0.38*RC
    - 10-90% Slew = 0.9*RC

Design Rules of Thumb

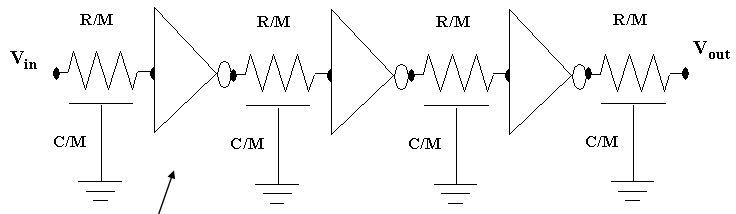
- RC delays should be considered when t_{pRC} is a sizable fraction of the unloaded gate delay (t_{pgate}) of the driver
- Ex: in our technology tpgate ~ 40-60ps (inverters)
- Resistance of a 500um line at 0.08 Ω/square:
- Cap: roughly 2pF/cm
- Need wires of length ~400um to have appreciable RC
- Also compare Rwire to Req of driver

How to reduce RC delay

- Since RC delay is quadratic with length, reducing length is key
- Note: $2^2 = 4$ and $1+1 = 2$ but $1^2 + 1^2 = 2$



Repeaters

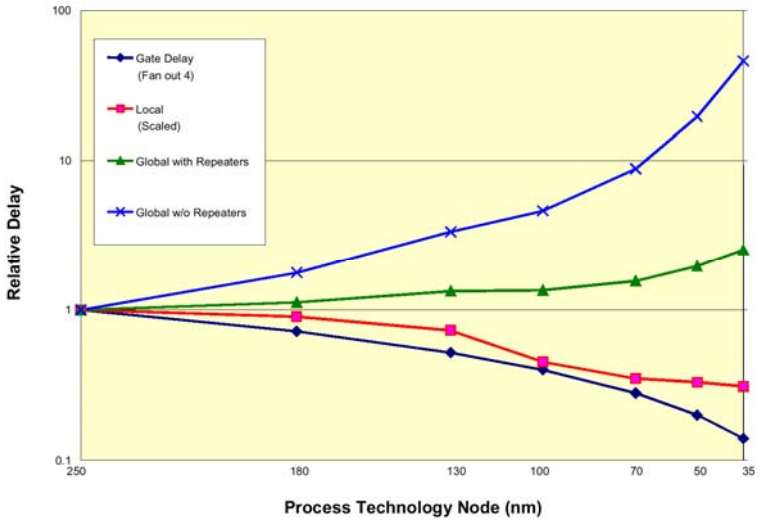


Repeater

Repeater = strong driver (usually an inverter or pair of inverters for non-inverting polarity) placed along a long RC line to "break up" the line and reduce delay

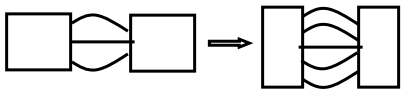
We need to determine optimal # of repeaters and their size based on wire and device delay properties

Repeaters Impact

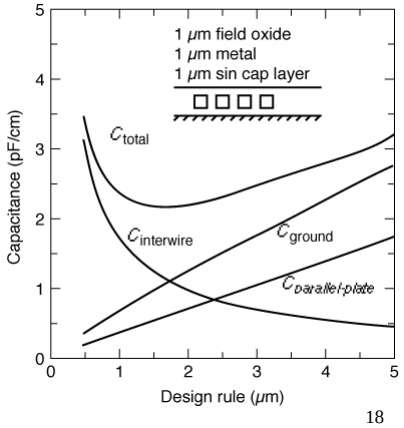


Coupling Capacitance

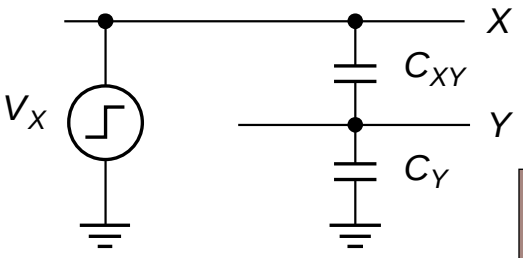
- To reduce interconnect resistance, thickness is not scaled as aggressively as the width of the interconnect



- Tall wires (high aspect ratios)

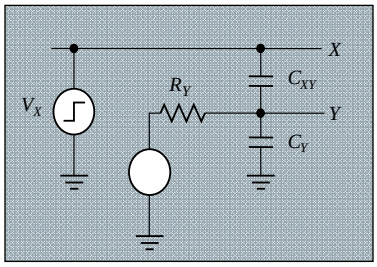


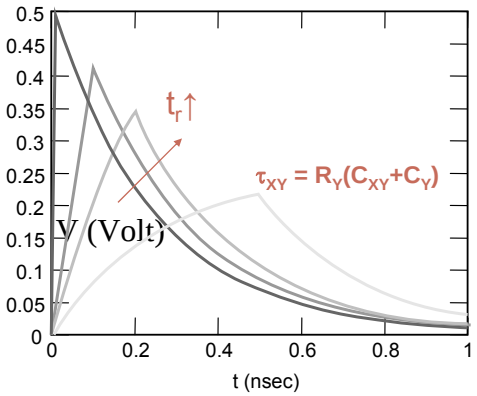
Capacitive Cross Talk



$$\Delta V_Y = \frac{C_{XY}}{C_Y + C_{XY}} \Delta V_X$$

Capacitive Cross Talk



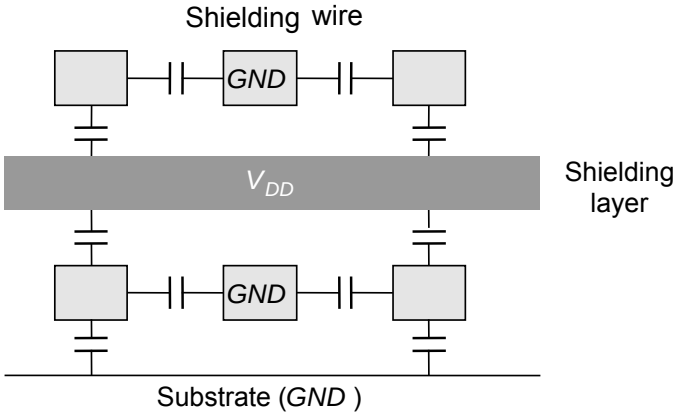


Keep time-constant small (size up driver of node Y)

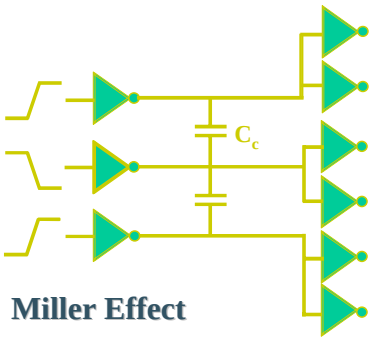
Dealing with Capacitive Cross Talk

- Avoid floating nodes (keepers!)
- Protect sensitive nodes (keep wires short)
- Make rise and fall times as large as possible
- Do not run wires together for a long distance
- Use shielding wires
- Use shielding layers

Shielding



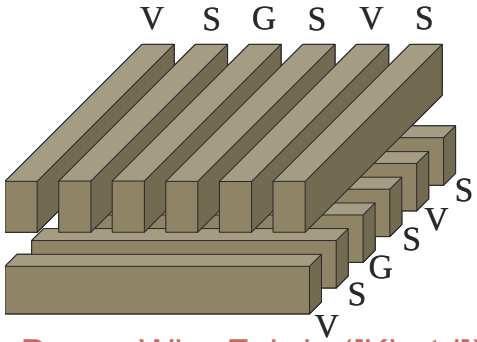
Impact of Crosstalk on Delay



DELAY DEPENDENT UPON ACTIVITY IN NEIGHBORING WIRES! (very important today)

- Both terminals of capacitor are switched in opposite directions ($0 \rightarrow V_{dd}$, $V_{dd} \rightarrow 0$)
- Effective voltage is doubled and additional charge is needed (from Q=CV)

Structured Predictable Interconnect

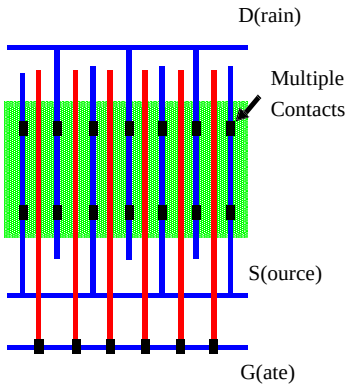


Example: Dense Wire Fabric ([Khatri])

Trade-off:

- Cross-coupling capacitance 40x lower, 2% delay variation
- Large increase in area and overall capacitance

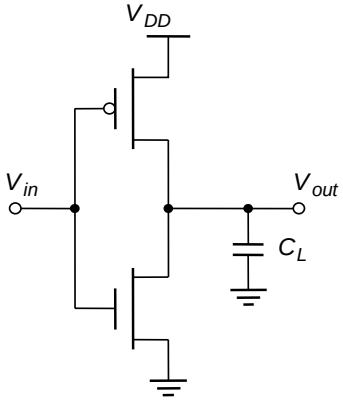
How to Design Large Transistors



Reduces diffusion capacitance
Reduces gate resistance

Many small transistors in parallel

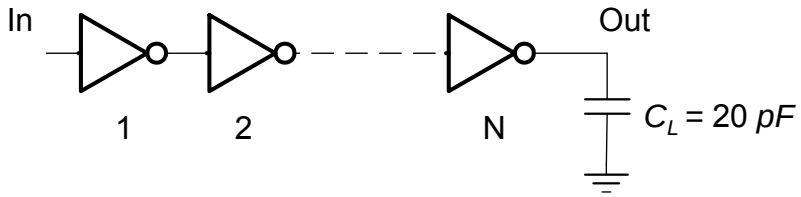
Driving Large Capacitances



$$t_p = \frac{C_L V_{swing}}{I_{av}}$$

- Transistor Sizing
- Cascaded Buffers

Using Cascaded Buffers

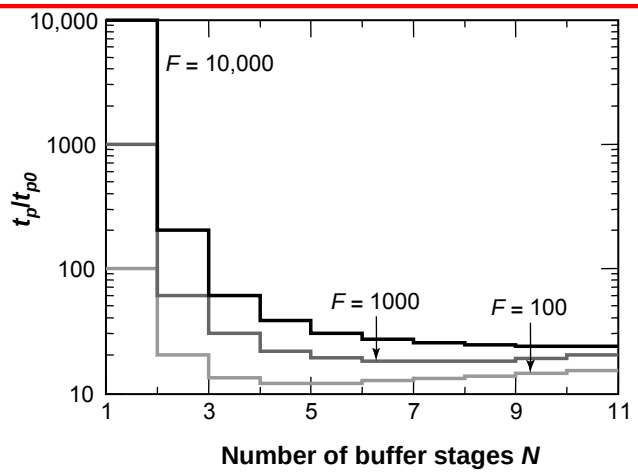


0.25 µm process
Cin* = 2.5 *fF
tp*0 = 30 *ps

***F* = *CL*/*Cin* = 8000**
***fopt* = 3.6 *N* = 7**
tp* = 0.76 *ns

(See Section 5.4)

Delay as a Function of F and N



Output Driver Design

0.25 μm process, C_L = 20 pF

Transistor Sizes for optimally-sized cascaded buffer t_p = 0.76 *ns*

Stage	1	2	3	4	5	6	7
W_n (μm)	0.375	1.35	4.86	17.5	63	226.8	816.5
W_p (μm)	0.71	2.56	9.2	33.1	119.2	429.3	1545.5

Transistor Sizes of redesigned cascaded buffer t_p = 1.8 *ns*

Stage	1	2	3
W_n (μm)	0.375	7.5	150
W_p (μm)	0.71	14.4	284

Repeaters vs. Cascaded Buffer Chains

- Repeaters are used to drive long RC lines
  - Breaking up quadratic dependence of delay on line length is the goal
  - Typically sized identically
- Cascaded buffers are used to drive large capacitive loads, where there is no parasitic resistance
  - We put all buffers at the beginning of the load
  - This would be pointless for a long RC wire since the wire RC delay would be unaffected and dominate the total delay

Summary

- Wires provide connectivity but also pose delay, noise, power problems
- Long wires can be partitioned using repeaters
- Coupling capacitance impacts both delay and noise; delay more critical
- Can cascade inverters to drive a large capacitive load like an I/O pad
  - Size each gate 3 or 4 times bigger than the last
- Next time: project discussion + getting started on logical effort