EECS 427
Lecture 5: Interconnect review
Reading: 4.3.1, 4.3.2, 4.4.1-4.4.3, 9.3.3

Last Time

• Power/energy in CMOS
  – Sources we will focus on are dynamic (caps) and leakage (subthreshold currents)
  – Much more later in the class on low-power design techniques
• Dynamic logic
  – Used sparingly, when speed is critical
  – Increases power, design complexity, poor noise properties compared to CMOS
  – Revisit today
Overview

• Wiring or interconnections and their performance impact
  – Contribute to delay, RC
  – Coupling capacitance between wires
• Design strategies to deal with large RC or C delays
  – Repeaters and cascaded/tapered buffer chains

Monotonicity

• Dynamic gates require *monotonically rising* inputs during evaluation
  – 0 -> 0
  – 0 -> 1
  – 1 -> 1
  – But not 1 -> 0
Monotonicity Woes

• But dynamic gates produce monotonically falling outputs during evaluation
• Illegal for one dynamic gate to drive another!

\[ A = 1 \]

\[ \phi \quad \text{Precharge} \quad \text{Evaluate} \quad \text{Precharge} \]

\[ \hat{Y} \quad X \quad \hat{Y} \quad X \]

\[ \text{Y should rise but cannot} \]
Domino Gates

- Follow dynamic stage with inverting static gate
  - Dynamic / static pair is called domino gate
  - Produces monotonic outputs

Domino Optimizations

- Each domino gate triggers next one, like a string of dominos toppling over
- Gates evaluate sequentially but precharge in parallel
- Thus evaluation is more critical than precharge
- Skewed static stages can perform added logic
Keepers: A must-have

- Keeper helps with charge leakage, charge sharing
  - But – fights evaluation initially
- Must be kept very weak; often use $L > L_{min}$ and $W = W_{min}$
- Avoid truly floating nodes!

Transistors vs. Wires

- Cross section of modern technology is mostly dominated by wires.
**Reverse Scaling** of Interconnects

- Gate delays reduce with technology scaling
- Global interconnect delays increase with scaling
  - Interconnects must be included in analysis and optimization

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**Interconnect Parasitics**

- Classes of parasitics
  - Capacitance
  - Resistance
  - Inductance (627 focuses on this)
- Impact of interconnect parasitics
  - Increases propagation delay
  - Energy dissipation and power distribution
  - Reliability and signal integrity
Interconnect Modeling

- Lumped capacitance model is what we use for device/gate analysis

- Lumped RC model
  - For simple one segment RC:
    - 50% Delay = 0.69*RC
    - 10-90% Slew = 2.2*RC

- Distributed RC line model
  - More accurate for interconnect analysis
    - 50% Delay = 0.38*RC
    - 10-90% Slew = 0.9*RC

Design Rules of Thumb

- RC delays should be considered when $t_{pRC}$ is a sizable fraction of the unloaded gate delay ($t_{pgate}$) of the driver
- Ex: in our technology $t_{pgate}$ ~ 40-60ps (inverters)
- Resistance of a 500um line at 0.08 Ω/square:
- Cap: roughly 2pF/cm
- Need wires of length ~400um to have appreciable RC
- Also compare Rwire to Req of driver
How to reduce RC delay

• Since RC delay is quadratic with length, reducing length is key
• Note: \(2^2 = 4\) and \(1+1 = 2\) but \(1^2 + 1^2 = 2\)

Repeater = strong driver (usually an inverter or pair of inverters for non-inverting polarity) placed along a long RC line to “break up” the line and reduce delay

We need to determine optimal # of repeaters and their size based on wire and device delay properties
Repeaters Impact

- To reduce interconnect resistance, thickness is not scaled as aggressively as the width of the interconnect
- Tall wires (high aspect ratios)

Coupling Capacitance

- To reduce interconnect resistance, thickness is not scaled as aggressively as the width of the interconnect
- Tall wires (high aspect ratios)
Capacitive Cross Talk

\[ \Delta V_Y = \frac{C_{XY}}{C_Y + C_{XY}} \Delta V_X \]

Keep time-constant small (size up driver of node Y)
Dealing with Capacitive Cross Talk

- Avoid floating nodes (keepers!)
- Protect sensitive nodes (keep wires short)
- Make rise and fall times as large as possible
- Do not run wires together for a long distance
- Use shielding wires
- Use shielding layers

Shielding

Shielding wire

Shielding layer

Substrate (GND)

V_{DD}
Impact of Crosstalk on Delay

**Miller Effect**

- Both terminals of capacitor are switched in opposite directions
  \( 0 \rightarrow V_{dd}, V_{dd} \rightarrow 0 \)
- Effective voltage is doubled and additional charge is needed
  (from \( Q = CV \))

Structured Predictable Interconnect

- Example: Dense Wire Fabric ([Khatri])

**Trade-off:**
- Cross-coupling capacitance 40x lower, 2% delay variation
- Large increase in area and overall capacitance
How to Design Large Transistors

- Multiple Contacts
- Reduces diffusion capacitance
- Reduces gate resistance

Many small transistors in parallel

Driving Large Capacitances

- Transistor Sizing
- Cascaded Buffers

\[ t_p = \frac{C_L V_{\text{swing}}}{I_{av}} \]
Using Cascaded Buffers

\[ C_L = 20 \text{ pF} \]

\begin{align*}
0.25 \mu\text{m process} & \quad F = C_L/C_{in} = 8000 \\
C_{in} = 2.5 \text{ fF} & \quad f_{opt} = 3.6 \quad N = 7 \\
tp_0 = 30 \text{ ps} & \quad tp = 0.76 \text{ ns}
\end{align*}

(See Section 5.4)

Delay as a Function of F and N

\begin{align*}
\frac{t_p}{tp_0} & \quad \text{Number of buffer stages } N
\end{align*}
Output Driver Design

0.25 μm process, $C_L = 20 \text{ pF}$

Transistor Sizes for optimally-sized cascaded buffer $t_p = 0.76 \text{ ns}$

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_p$ (μm)</td>
<td>0.375</td>
<td>1.35</td>
<td>4.86</td>
<td>17.5</td>
<td>63</td>
<td>226.8</td>
<td>816.5</td>
</tr>
<tr>
<td>$W_n$ (μm)</td>
<td>0.71</td>
<td>2.56</td>
<td>9.2</td>
<td>33.1</td>
<td>119.2</td>
<td>429.3</td>
<td>1545.5</td>
</tr>
</tbody>
</table>

Transistor Sizes of redesigned cascaded buffer $t_p = 1.8 \text{ ns}$

<table>
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<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_p$ (μm)</td>
<td>0.375</td>
<td>7.5</td>
<td>150</td>
</tr>
<tr>
<td>$W_n$ (μm)</td>
<td>0.71</td>
<td>14.4</td>
<td>284</td>
</tr>
</tbody>
</table>

Receivers vs. Cascaded Buffer Chains

- Repeaters are used to drive long RC lines
  - Breaking up quadratic dependence of delay on line length is the goal
  - Typically sized identically
- Cascaded buffers are used to drive large capacitive loads, where there is no parasitic resistance
  - We put all buffers at the beginning of the load
  - This would be pointless for a long RC wire since the wire RC delay would be unaffected and dominate the total delay
Summary

• Wires provide connectivity but also pose delay, noise, power problems
• Long wires can be partitioned using **repeaters**
• Coupling capacitance impacts both delay and noise; delay more critical
• Can cascade inverters to drive a large capacitive load like an I/O pad
  – Size each gate 3 or 4 times bigger than the last
• Next time: project discussion + getting started on logical effort