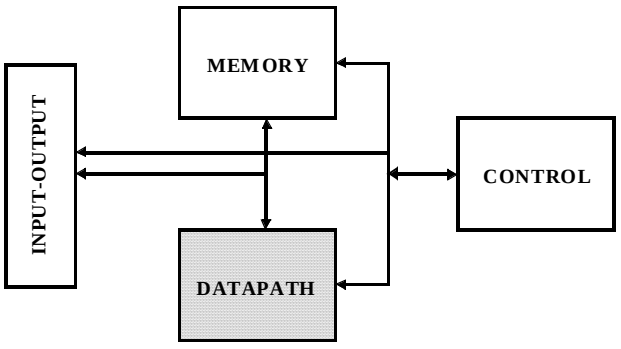
EECS 427
Lecture 8: Intro to adders
Reading: 11.1 – 11.3.1

A Generic Digital Processor



Building Blocks for Digital Architectures

Arithmetic unit

- Bit-sliced datapath (adder, multiplier, shifter, comparator, etc.)

Memory

- RAM, ROM, Buffers, Shift registers

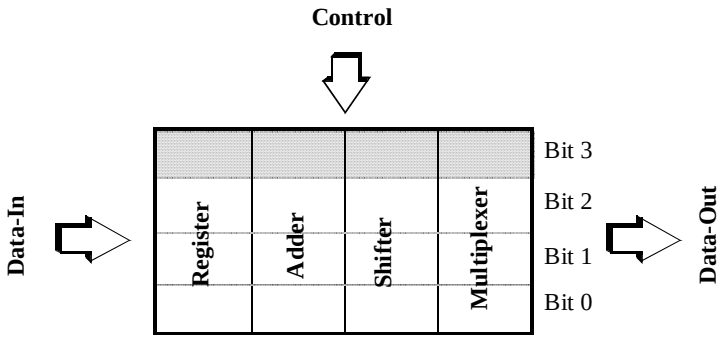
Control

- Finite state machine (PLA, random logic)
- Counters

Interconnect

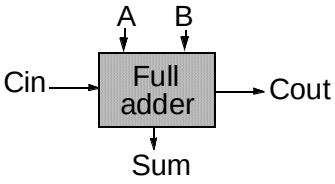
- Switches
- Arbiters
- Bus

Bit-Sliced Design



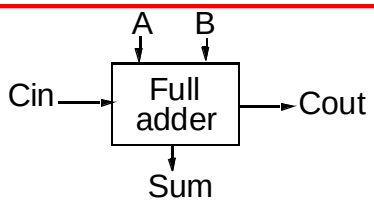
Tile identical processing elements

Full Adder



A	B	C_i	S	C_o	*Carry status*
0	0	0	0	0	delete
0	0	1	1	0	delete
0	1	0	1	0	propagate
0	1	1	0	1	propagate
1	0	0	1	0	propagate
1	0	1	0	1	propagate
1	1	0	0	1	generate
1	1	1	1	1	generate

The Binary Adder



$$S = A \oplus B \oplus C_i$$

$$= A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i + ABC_i$$

$$C_o = AB + BC_i + AC_i$$

Express Sum and Carry as function of P, G, D

Define 3 new variables that ONLY depend on A, B WHY?

Generate (G) = AB

Propagate (P) = A ⊕ B

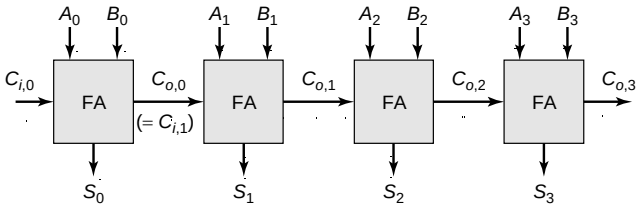
Delete = $\overline{A}\,\overline{B}$

$$C_o(G,P) = G + PC_i$$

$$S(G,P) = P \oplus C_i$$

Can also derive expressions for *S* and C_o based on *D* and *P*

The Ripple-Carry Adder



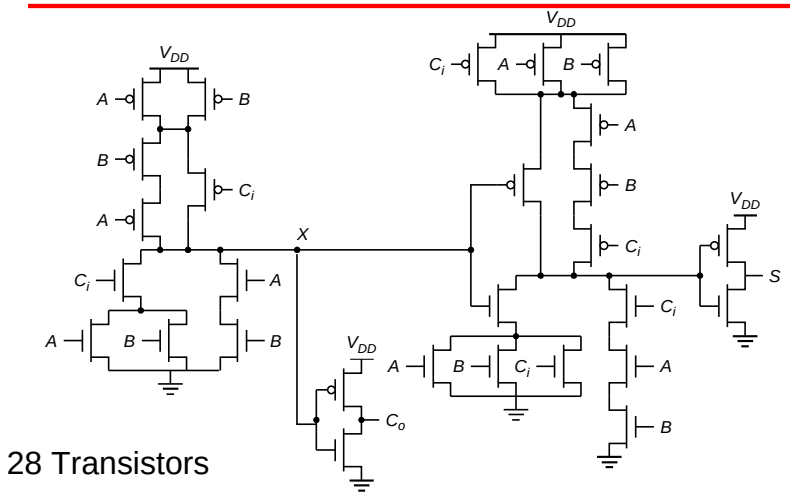
Worst case delay linear with the number of bits

$t_d = O(N)$

$t_{adder} = (N\text{-}1)t_{carry} + t_{sum}$

Goal: Make the fastest possible carry path circuit

Complementary Static CMOS Full Adder



28 Transistors

Summary

- Adders are a critical part of any digital processor
  - Adder design requires an architecture/topology (ex: ripple carry) and a bit cell design (ex: std. static CMOS)
  - More architectures and cell designs next time