

The University of Michigan
Department of Electrical Engineering and Computer Science
EECS 427 Fall 2008
Quiz 1

Name: _____ **UM ID:** _____

For full credit, show the pertinent work leading to your answers

Problem #	Maximum Possible Points	Obtained Points
1	22	
2	12	
3	10	
4	16	
5	20	
6	20	
Total	100	

I have neither given nor received any unauthorized aid during this exam

Signed: _____

1.0 Problem 1 (22 Points) – Logical Effort & Tapering

Consider the circuit shown in Figure 1. Assume that the effective P/N ratios of all gates is 3 and a P/N ratio of 3 in an inverter results in equal rise and fall delays. The intrinsic delay of an inverter $p_{inv} = 1\tau$. Assume that the branch gates G and H are sized for equal stage effort with their corresponding on-path gate, D (and they have the same total output capacitance). Note that the 2-input NAND gates, C and D, have tapered NMOS stacks while all other gates are *NOT* tapered (including the 2-input NAND gate within the AND macro cell). Finally, note that the inverter and NAND gate inside the macro cell have a fixed size ratio relative to each other.

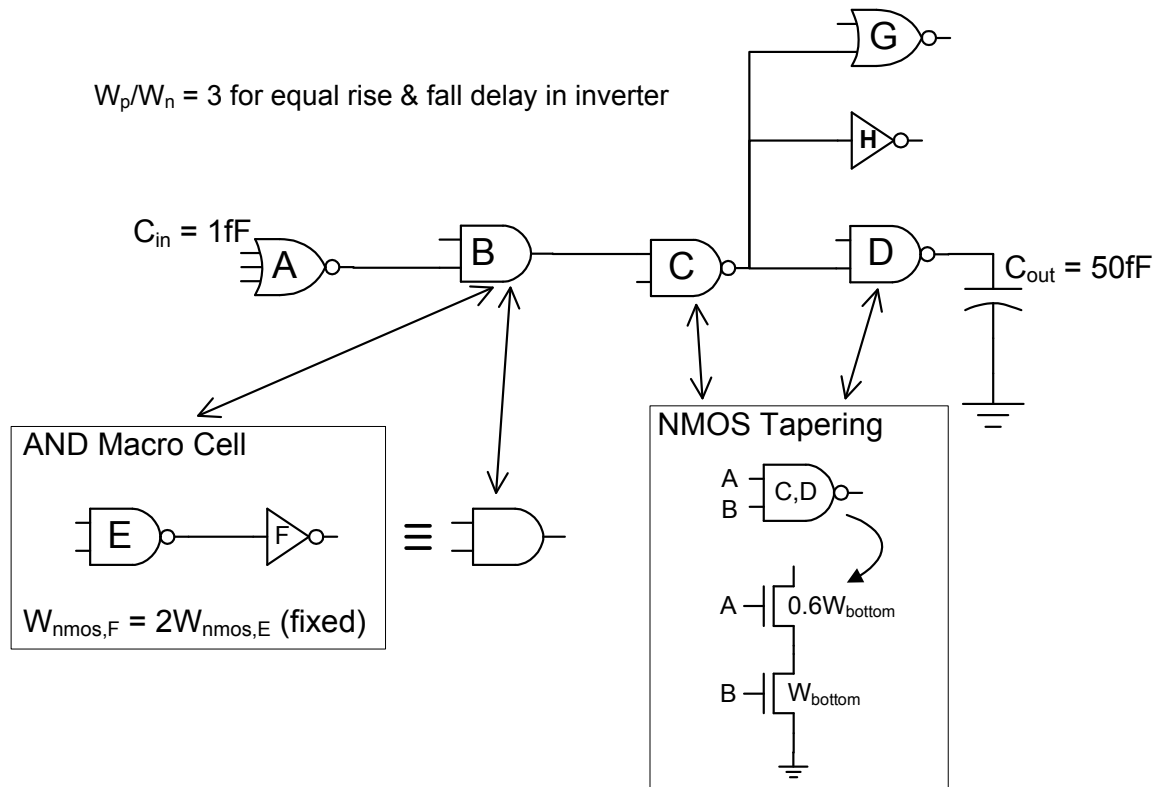


Figure 1. Circuit for Problem 1.0.

1.1 (10 Points) Fill in the table below, calculating the intrinsic delay, p , and the logical effort, g , for each gate. (Blank space is included on the following page for work.)

Table 1. Answer to Problem 1.1.

Gate Type	p	g
Inverter (H)		
Nor2 (G)		
Nand2 (D)		
Nand2 (C)		
And (B)		
Nor3 (A)		

(Work for Problem 1.1.)

1.2 (4 Points) Find the path effort, F , for the path shown in Figure 1 and calculate the minimum delay using optimal gate sizing. Add extra inverters to the circuit to minimize the delay, if needed (refer to Table 2). Make sure the functionality of the circuit does not change.

Table 2. Table of ranges of path effort, F , and optimum stages, N .

N	F
1	0 - 5.83
2	5.84 - 22.3
3	22.4 - 82.2
4	82.3 - 300
5	301 - 1090
6	1091 - 3920
7	3921 - 14200

1.3 (4 Points) Compute the input capacitance of each of the gates A – D, as well as any inverters that you might have added, so that delay is minimum. Assume the gate capacitance of transistors, $C_{ox}=1\text{fF}/\mu\text{m}^2$ and the length of all the transistors to be $1\mu\text{m}$.

1.4 (4 Points) Calculate the corresponding NMOS and PMOS transistor sizes for each of the gates A – D.

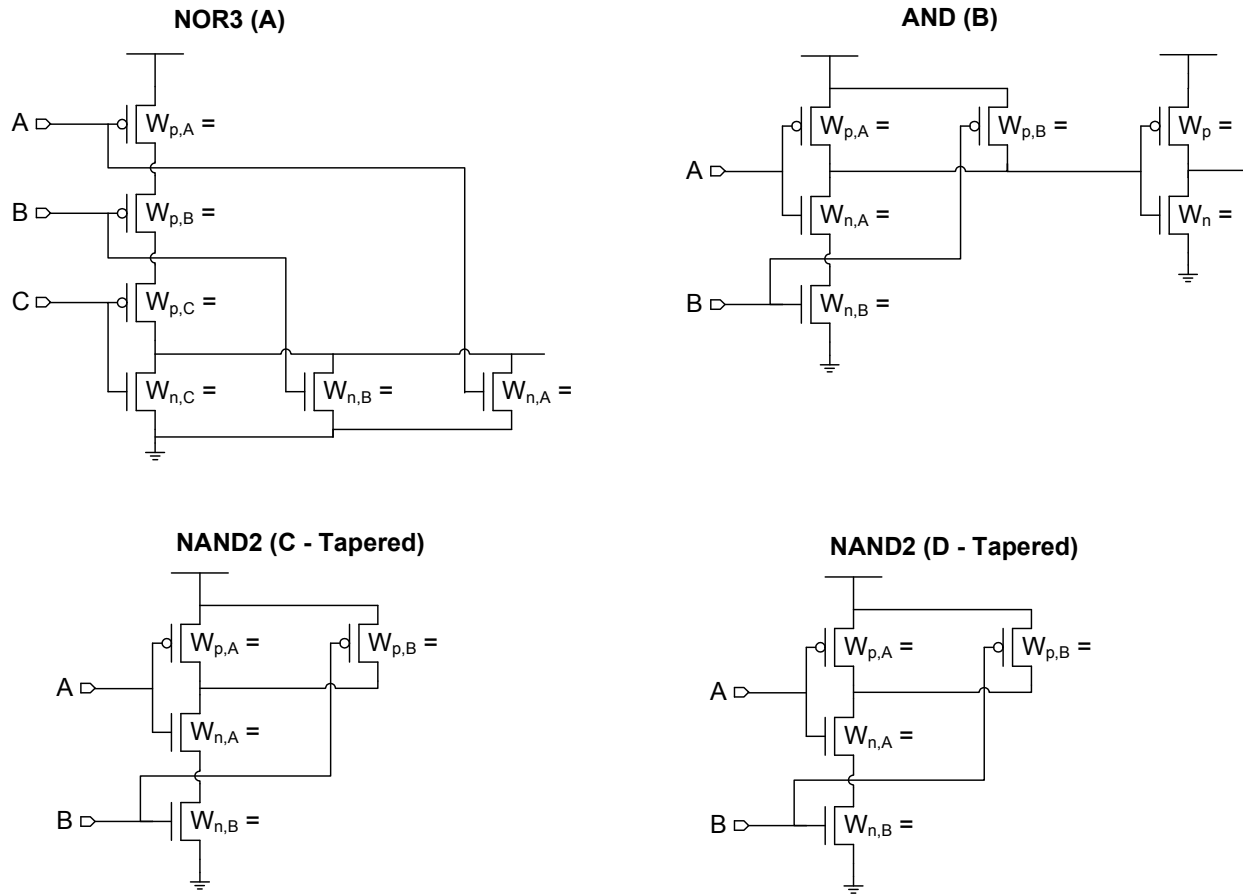


Figure 2. Answer to Problem 1.4.

2.0 Problem 2 (12 Points) – Layout

Given two primary inputs, A and sel , draw a stick diagram for the layout implementation for the tri-state inverter given by the truth table shown below in Table 3. Assume that the sel input is the latest arriving input and adjust your circuit and layout accordingly. Draw your diagram within Figure 3. Draw your transistor level circuit implementation below the layout.

Table 3. Truth table for Problem 2.0.

A	sel	Y
0	0	Z
0	1	V_{DD}
1	0	Z
1	1	0V

- * Z represents a high impedance state
- * Logic 0 represents 0V
- * Logic 1 represents V_{DD}

Important: Continuous diffusion regions for nfets and pfets, as well as metal 1 rails must remain as shown in Figure 3. In other words, you cannot change the M1, diffusion, and poly that is already shown in Figure 3. To implement the tri-state inverter, *you can only connect poly, add M1 or add contacts*. Show your poly connections, added metal routes and contacts in Figure 3 and label your inputs A , sel , and output Y .

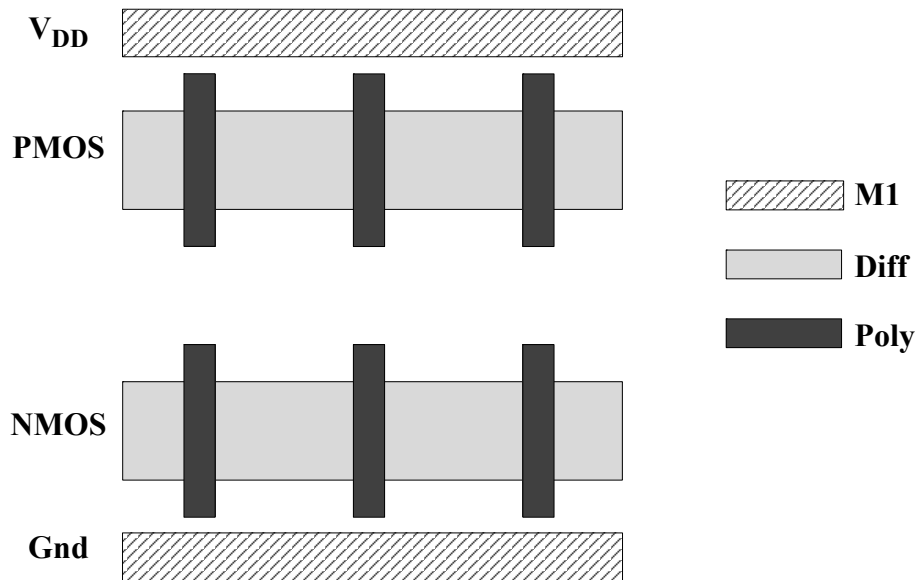


Figure 3. Incomplete layout for Problem 2.0.

Transistor-level circuit implementation:

3.0 Problem 3 (10 Points) – Antenna Rules

3.1 Consider the routing layout between three inverters g1, g2, and g3, as shown in Figure 4. Answer the following questions.

(a) (4 Points) Which gate/gates (g1, g2, or g3) is/are the *most susceptible* to antenna violations?

(b) (3 Points) Which gate/gates (g1, g2, or g3) is/are the *least susceptible* to antenna violations?

(c) (3 Points) Add one reversed biased diode to one of the existing metal nets to fix the antenna problem(s). Draw the diode within Figure 4. Explain below why you chose the location of your diode. (An example diode connection to M1 is shown in the bottom left corner of Figure 4.)

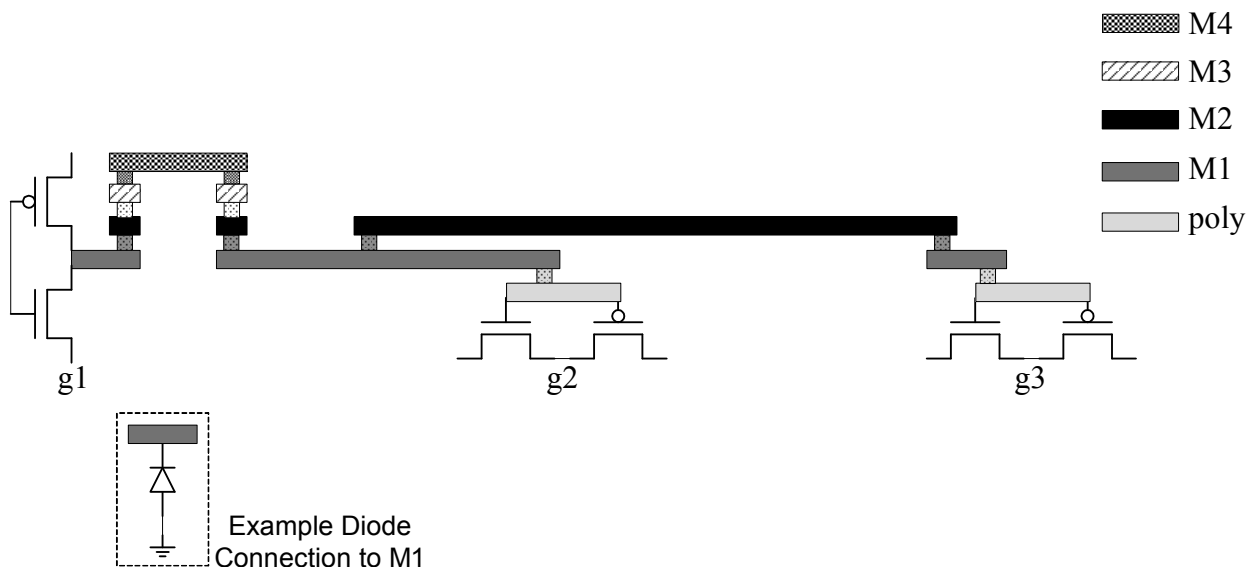


Figure 4. Circuit for Problem 3.0.

4.0 Problem 4 (16 Points) – Short Answer

Answer the following questions as briefly as possible. Use less than 4 sentences of explanation for each answer.

4.1 (2 Points) Explain why polysilicon was necessary for the development of a self-aligned process.

4.2 (2 Points) What is the approximate P/N ratio that provides equal rise and fall delays in an inverter for our $0.13\mu\text{m}$ process (used in the CAD assignments and discussed in lecture)?

4.3 (4 Points) List 2 current Resolution Enhancement Techniques (RETs) and in one sentence each, describe how they improve the lithography in modern processes.

4.4 (3 Points) Is transistor tapering more or less effective if the output capacitance of a gate is high? Explain.

4.5 (5 Points) – Use Figure 5 below to answer the next 2 questions about RET.

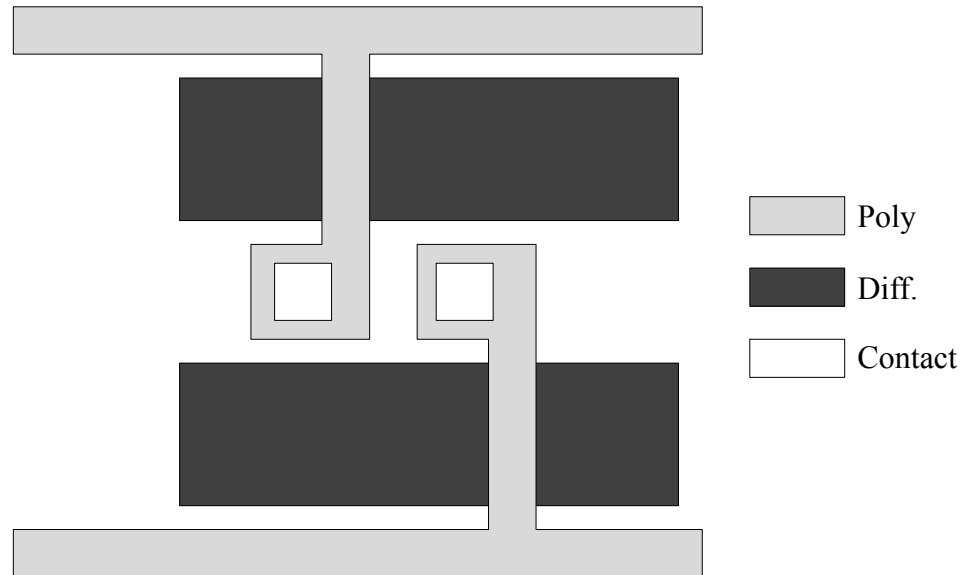


Figure 5. Layout for Problem 4.5.

- (a) In Figure 5 above, indicate where the *polysilicon* mask will differ from the layout by drawing serifs, notches, and/or hammerheads in the correct locations.
- (b) Which design rules will be affected by the changes made to Figure 5 and how (increase or decrease, e.g., “metal-metal spacing increases”, etc.)? Explain.

5.0 Problem 5 (20 Points) – Adders

5.1 (9 Points) All inputs to a 16-bit, 4-stage carry-bypass adder, shown in Figure 6, are initially zeros. What new inputs (all of which arrive simultaneously) result in a worst-case delay to the sum? Give the specific input vectors for C_{in} , $A<15:0>$, and $B<15:0>$. In your answer, indicate which bit is the least significant bit (LSB). Explain briefly why this is the worst-case input. If necessary, use the delays t_{setup} , t_{c_gen} , t_{p_block} , t_{mux} , and t_{sum} in your explanation.

(NOTE: There may be multiple correct answers.)

Assume that the 5 main delay values (t_{setup} , t_{c_gen} , t_{p_block} , t_{mux} , and t_{sum}) are all within 2-3X of each other.

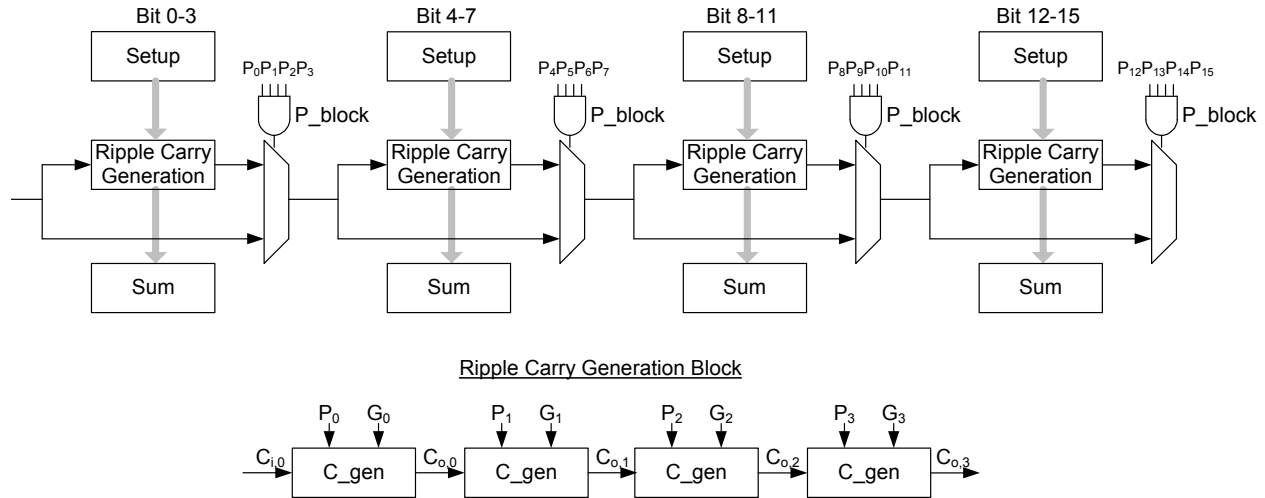


Figure 6. Carry bypass adder architecture used in Problem 5.0

Initial State:

$$C_{in} = 0$$

$$A = 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0$$

$$B = 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0$$

↑
LSB

Next State = ? (next state results in worst-case delay; don't forget to mark the LSB of your vector)

$$C_{in} =$$

$$A =$$

$$B =$$

Explanation:

5.2 (11 Points) Shown below are two subsequent input states to the same carry-bypass adder (from Figure 6). Determine the actual delay from the arrival of the new inputs to the final sum generation. Briefly show what the worst-case path is and explain why. Again, assume that all inputs arrive simultaneously. Express your answer as an equation utilizing t_{setup} , t_{c_gen} , t_{p_block} , t_{mux} , and t_{sum} . All LSB's (least significant bits) are on the left.

Initial input state:

$$C_{in} = 0$$

$$A = 1\ 1\ 0\ 0\ \quad 0\ 0\ 1\ 0\ \quad 1\ 0\ 0\ 1\ \quad 1\ 0\ 0\ 1$$

$$B = 0\ 1\ 0\ 1\ \quad 1\ 1\ 0\ 1\ \quad 0\ 0\ 0\ 0\ \quad 0\ 1\ 0\ 1$$

Next input state:

$$C_{in} = 0$$

$$A = 1\ 1\ 1\ 1\ \quad 0\ 0\ 1\ 0\ \quad 1\ 1\ 0\ 1\ \quad 0\ 1\ 0\ 1$$

$$B = 0\ 0\ 0\ 1\ \quad 1\ 1\ 1\ 1\ \quad 0\ 0\ 1\ 0\ \quad 1\ 0\ 0\ 1$$

6.0 Problem 6 (20 Points) – Sizing

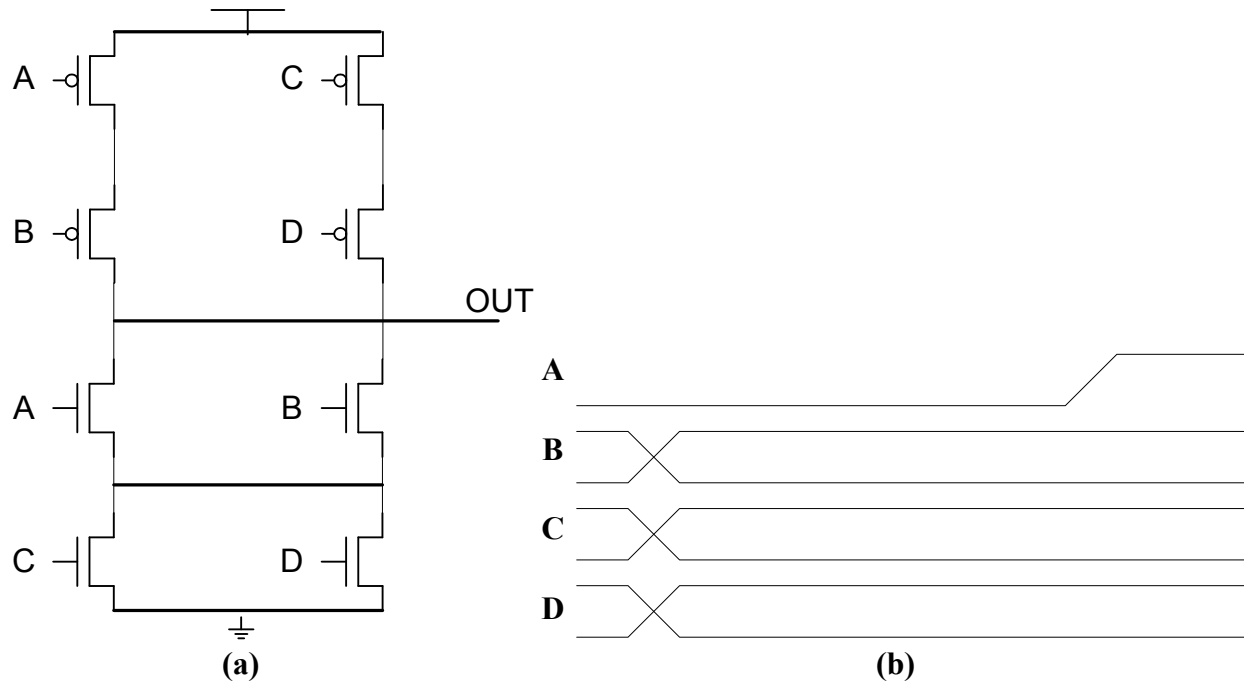


Figure 7. (a) Circuit for Problem 6.0.
(b) *Example Scenario 1* – Input A rises long after other inputs.

6.1 (9 Points) In the gate above, all transistors are equally sized. The load capacitance on ‘OUT’ is small, all inputs are stable, and the output is high. Under these conditions, consider four scenarios. In each, *only one input switches* (either A, B, C or D), which causes ‘OUT’ to get pulled to ground (i.e., the other inputs are stable and their values are set such that ‘OUT’ is connected to ground when the critical input goes high). Order the scenarios from shortest input-to-output delay to the longest input-to-output delay. Consider the worst case for each if multiple delays are possible for a scenario.

Table 4. Answer to Problem 6.1.

Scenario	Rank*
A (Input ‘A’ rises)	
B (Input ‘B’ rises)	
C (Input ‘C’ rises)	
D (Input ‘D’ rises)	

* A rank of “1” represents the shortest input-to-output delay, while “4” represents the longest.

6.2 (11 Points) Now, consider the scenario described in Problem 6.1 where input 'B' is the switching signal and all other inputs are not changing. Assign the transistors' sizes to minimize the fall delay for this scenario. For each of the transistors in the pull-up and pull-down networks, assign a width of 1-unit (the narrowest) to 4-units (the widest). All transistors have equal gate lengths. You should use each width of 1-, 2-, 3-, or 4-units exactly once each in the pull-up network, and exactly once each in the pull-down network. *Explain your choices* – in case of ambiguity, explain why one choice might be better than another or not. (Please write your sizings directly next to the transistors in the circuit diagram in Figure 7a).