The University of Michigan
Department of Electrical Engineering and Computer Science

EECS 427 Fall 2008

Quiz 2

Name:______________________ **UM ID:**_________________

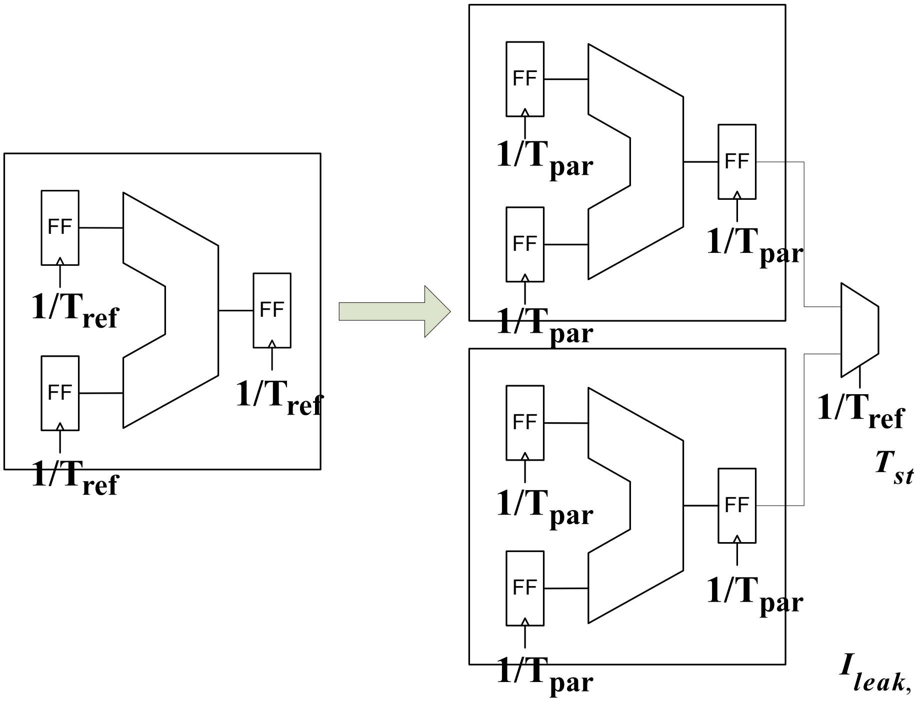
For full credit, show the pertinent work leading to your answers

Problem #	Maximum Possible Points	Points Obtained
1	19	
2	8	
3	13	
4	12	
5	19	
6	6	
7	6	
8	17	
Total	100	

I have neither given nor received any unauthorized aid during this exam

Signed: ____________________________

1.0 Problem 1 (19 Points) – Parallelism



$$T_{stage} = T_0 \frac{V_{DD}}{(V_{DD} - V_{th})^2}$$

$$I_{leak,\,stage} = I_0 e^{\left(\frac{V_{gs} - V_{th}}{nV_T}\right)}$$

(a) Singe Execution Stage (Ref) (b) Parallel Execution Stage (Par) (c) Useful Equations

Figure 1. Circuit for Problem 1.0.

Circuit Parameters: T_0 = 1x10^{-9} s•V$^{0.5}$; $V_{DD,ref}$ = 1.2V; V_{th} = 0.4V; total switching capacitance of one single execution stage, C_{tot} = 200fF; switching activity (avg. # of high-to-low or low-to-high transitions in one clock cycle), α = 0.2; n = 1; V_T = 26mV; C_{mux} = 20fF; I_0 = 60A.

During the early stages of a block design, a designer determines that there are two possible implementations of the circuit, shown in Figure 1a and Figure 1b. The area specifications for the design allow for either a single execution stage (Figure 1a) or a 2-way parallel execution stage (Figure 1b). Both implementations must result in the *same* throughput. **Use the equations shown in Figure 1c in your answers to the following questions.**

1.1 (4 Points) What supply voltage, $V_{DD,par}$, can the 2-way parallel implementation operate at? Ignore the additional delay added by the mux in the 2-way parallel case.

$V_{DD,par}$ = ?

1.2 (6 Points) What is the gain/loss in total power of the parallel implementation, $P_{total,par}$, relative to the original power, $P_{total,ref}$? Consider both leakage and dynamic power. Ignore the additional leakage added by the mux in the 2-way parallel case.

$$\frac{P_{total,par}}{P_{total,ref}} = ?$$

1.3 (5 Points) A designer decides to exploit as much parallelism as possible while maintaining constant throughput. As the number of parallel execution units approach ∞, describe the following **four** quantities:

1. V_{DD,par_∞} =

2. P_{Dyn,par_∞} =

3. P_{leak,par_∞} =

4. Total power, P_{total,par_∞} relative to P_{ref}. Is it: more, less, equal (circle one)

Explain.

1.4 (4 Points) Consider a different execution stage than the one described by the parameters in this problem. You find that with this execution stage, a parallelism of 2 has higher power than a parallelism of 1. *List at least three parameters* that could have caused this higher power and *whether these parameters would have been higher or lower than in the original case* in Problem 1.1.

2.0 Problem 2 (8 Points) – Dynamic Logic Techniques

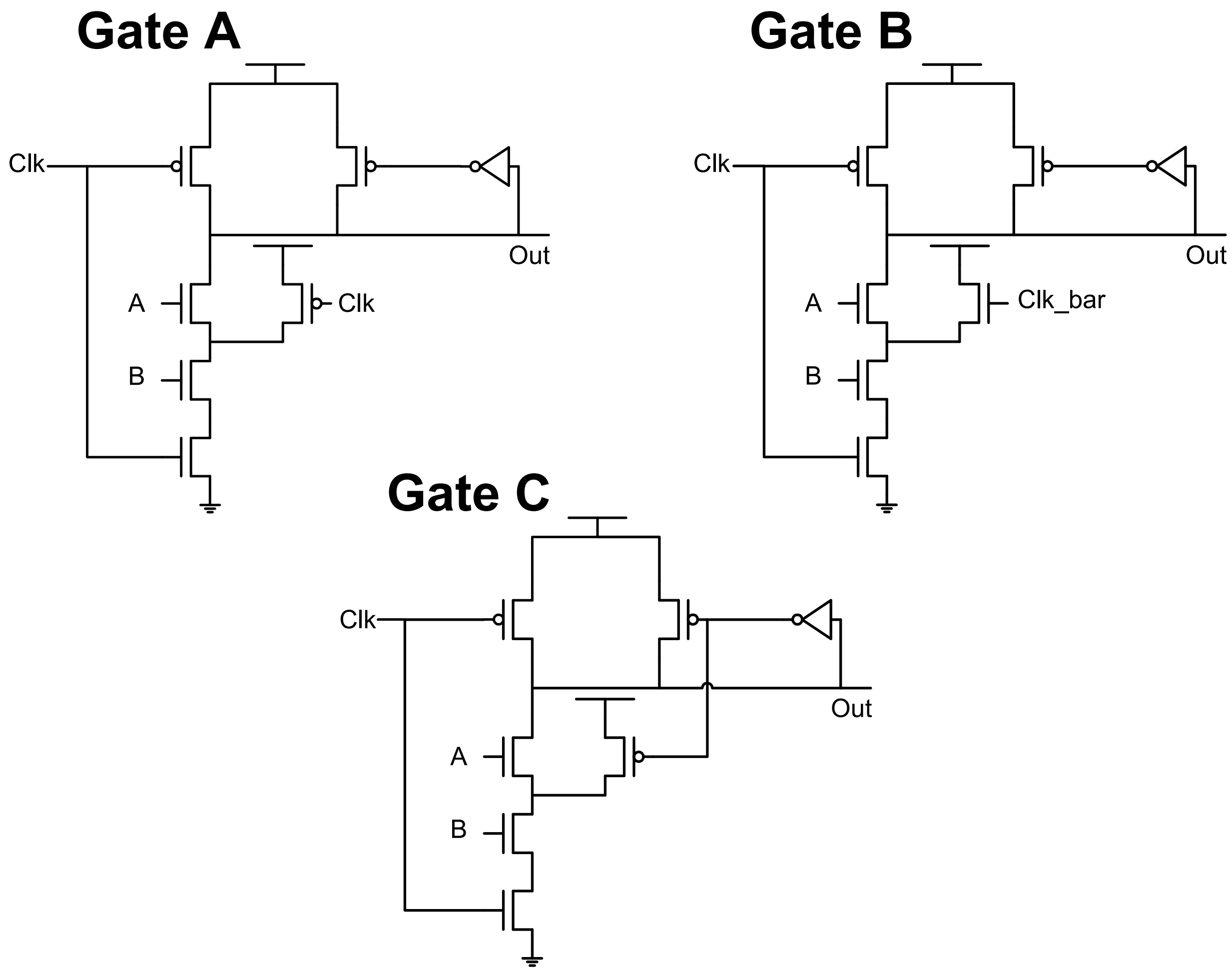


Figure 2. Three dynamic logic gates for Problem 2.0.

Presented are three variations of a dynamic 2-input NAND gate. *Please order them in robustness and speed.* **Explain briefly below.**

SPEED		**ROBUSTNESS**	
Fastest	________	Most Robust	________
Medium	________	Medium	________
Slowest	________	Least Robust	________

Explain:

3.0 Problem 3 (13 Points) – Process Variation

Below are two logic cones in the same circuit. Assume that without process variation, all gates have the same delay, and interconnect delays are equal. Also, assume that the only source of variation in gate delay is from variation in threshold voltage, V_{th}. Finally, assume that the AND gates are not affected by variation.

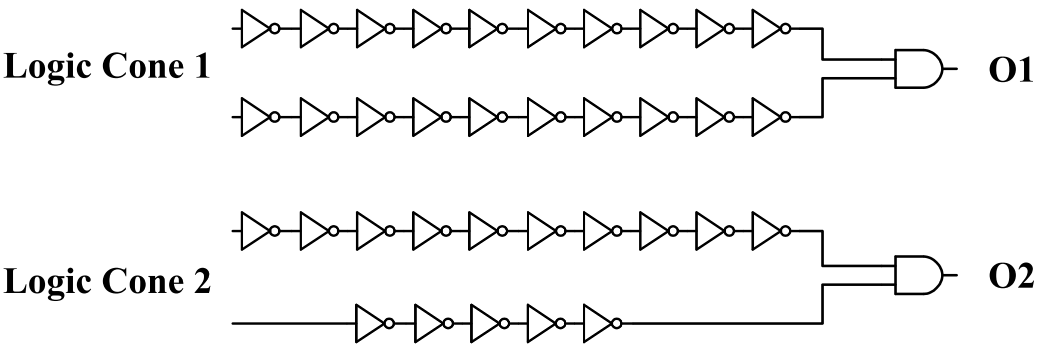


Figure 3. Two logic cones under examination in Problem 3.0.

a) **(4 Points)** If **V_{th} variation is uncorrelated**, which output (O1 or O2) is expected to have worse **99th percentile delay**, or are the 99th percentile delays equal? **Explain.**

b) **(4 Points)** If **V_{th} variation is instead perfectly correlated** within a die, which group is expected to have worse 99th percentile delay, or are 99th percentile delays equal? **Explain.**

c) **(5 Points)** Consider the following four scenarios where each considers one output/logic cone and either correlated or uncorrelated variation. Please order the scenarios from largest to smallest sigma of output transition time in *absolute* terms.

Scenario 1: Output O1, logic cone 1: V_{th} variation is uncorrelated

Scenario 2: Output O2, logic cone 2: V_{th} variation is uncorrelated

Scenario 3: Output O1, logic cone 1: V_{th} variation is perfectly correlated

Scenario 4: Output O2, logic cone 2: V_{th} variation is perfectly correlated

	Scenario Number
Largest sigma	_______
	_______
	_______
Smallest sigma	_______

4.0 Problem 4 (12 Points) – SRAM

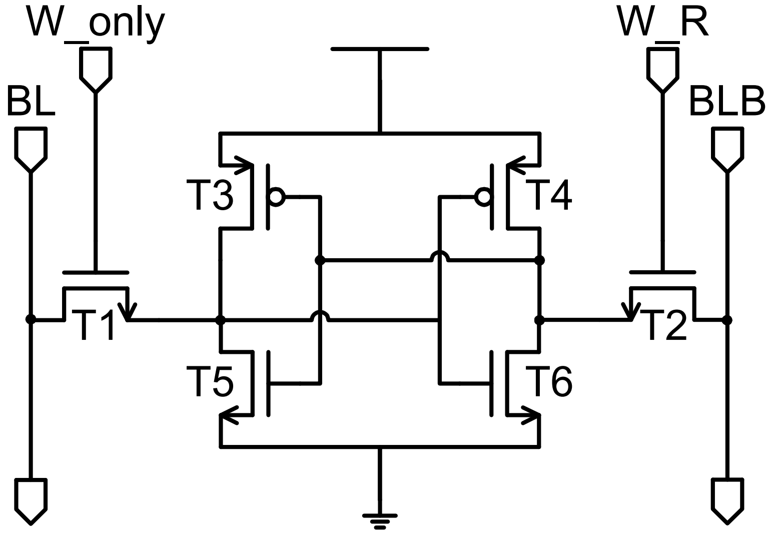


Figure 4. SRAM Circuit for Problem 4.0.

The circuit above is similar to a traditional 6T-SRAM with **one major difference**:on a write, **both** *W_only* and *W_R* go high (writing the SRAM from both sides); on a read, **only** *W_R* goes high, reading the value onto *BLB*.

4.1 (4 Points) How would you modify transistors T1 – T6 to test for **write robustness**? **Assume only V_{th} variation matters**. For each transistor in Figure 5 below, circle the correct value to skew V_{th} by, either -3σ or +3σ to test for worst case robustness.

NOTE: Notice the existing node voltages within the SRAM, as well as the values we're trying to write.

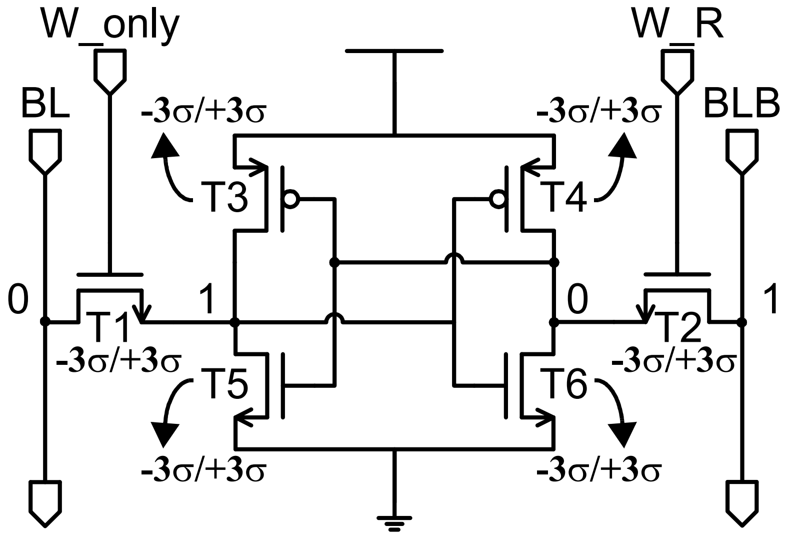


Figure 5. SRAM Circuit for Problem 4.1.

4.2 (4 Points) How would you modify transistors T1 – T6 to test for **read robustness**? Similar to Problem 4.1, for each transistor in Figure 6 below, circle the correct value to skew V_{th} by, either -3σ or +3σ to test for worst case robustness.

NOTE: The internal node voltages of the SRAM cell are the same as Problem 4.1.

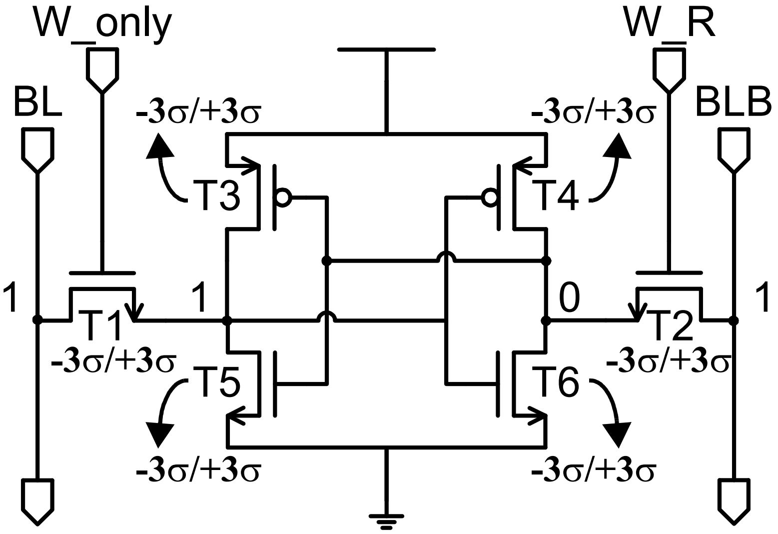


Figure 6. SRAM Circuit for Problem 4.2.

4.3 (4 Points) While sizing the SRAM cell from Figure 4 for robustness, what will the relative transistor sizings be for transistor pairs [T1,T2] and [T5,T6]. **Fill in the blanks below (fill in "greater than," "less than," or "equal" between pairs)**. **Explain**.

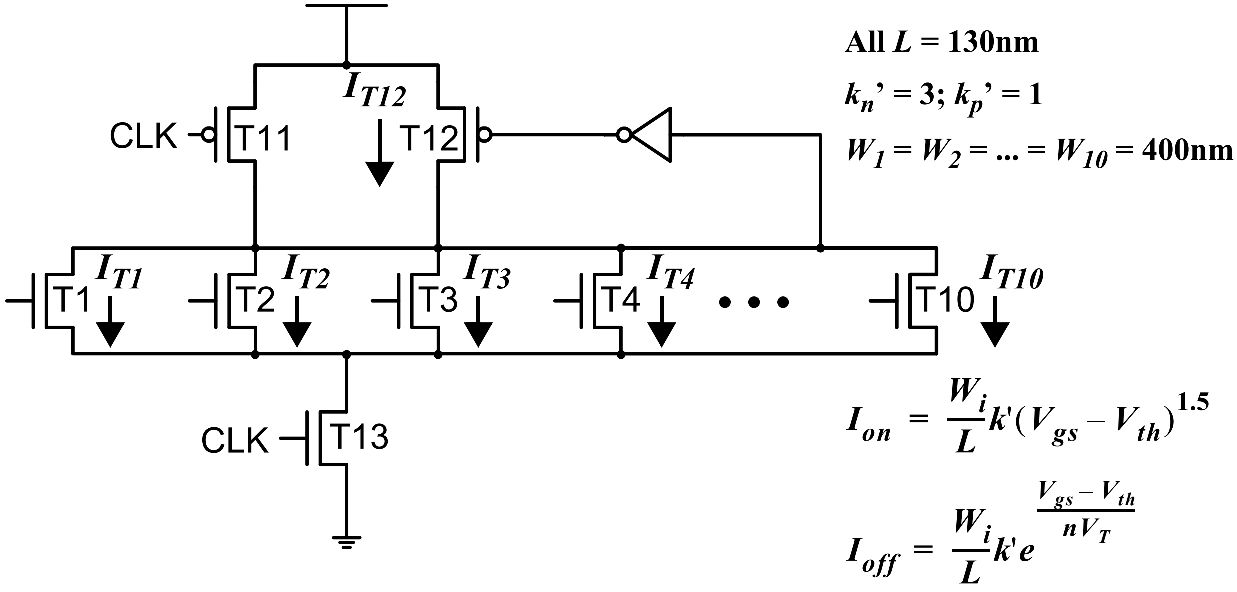
(e.g., T3 greater than T4)

T1 ________________ T2

T5 ________________ T6

Explain:

5.0 Problem 5 (19 Points) – Dynamic Logic Sizing & Robustness



All L = 130nm

k_n’ = 3; k_p’ = 1

$W_1 = W_2 = ... = W_{10}$ = 400nm

$$I_{on} = \frac{W_i}{L}k'(V_{gs} - V_{th})^{1.5}$$

$$I_{off} = \frac{W_i}{L}k'e^{\frac{V_{gs} - V_{th}}{nV_T}}$$

Figure 7. 10-input dynamic NOR gate with keeper for Problem 5.0.

Circuit Parameters: V_{DD} = 1.2V; $V_{th,n}$ = 0.4V; $V_{th,p}$ = -0.4V; n = 3.5; V_T = 26mV.

Consider the 10-input dynamic NOR gate shown in the figure above and use the information provided to answer the following questions.

5.1 (8 Points) Provide an *inequality* that constrains the sizing of W_{12} (the keeper’s gate width) during the *evaluation* phase of the clock, given that $W_1 = W_2 = ... = W_{10}$ = **400nm**.

- **Ignore the drive current through T_{13}.**
- **Ignore the leakage current through T_{11}.**

5.2 (11 Points) After performing the initial sizing analysis from Problem 5.1, the process engineers inform you of the die-to-die and within-die distributions of V_{th} variation (*the nominal* V_{th} *is still* $+0.4V$ and $-0.4V$ for NMOS and PMOS devices, respectively). They are as follows:

$[\mu_{die\text{-}to\text{-}die}, \sigma_{die\text{-}to\text{-}die}] = [0, 40\text{mV}]$

$[\mu_{within\text{-}die}, \sigma_{within\text{-}die}] = [0, 30\text{mV}]$

NOTE: The within-die variation is perfectly *independent and uncorrelated.*

Assuming that V_{th} is the only type of variation, *will your sizes from Problem 5.1* still work with worst case ($\pm 3\sigma$) variation considering:

(1) die-to-die variation (D2D), only

(2) both die-to-die variation (D2D) and within-die variation (WD)?

(5 Points) **Scenario 1 (D2D, only): Circuit will (work/not work) ____________________**

Explain:

(6 Points) **Scenario 2 (D2D + WD): Circuit will (work/not work) ____________________**

Explain:

6.0 Problem 6 (6 Points) – Problems in High-Power Design

List three of the major problems that are introduced by having a very high-power chip design.

1)

2)

3)

7.0 Problem 7 (6 Points) – Verilog

Consider the following verilog module:

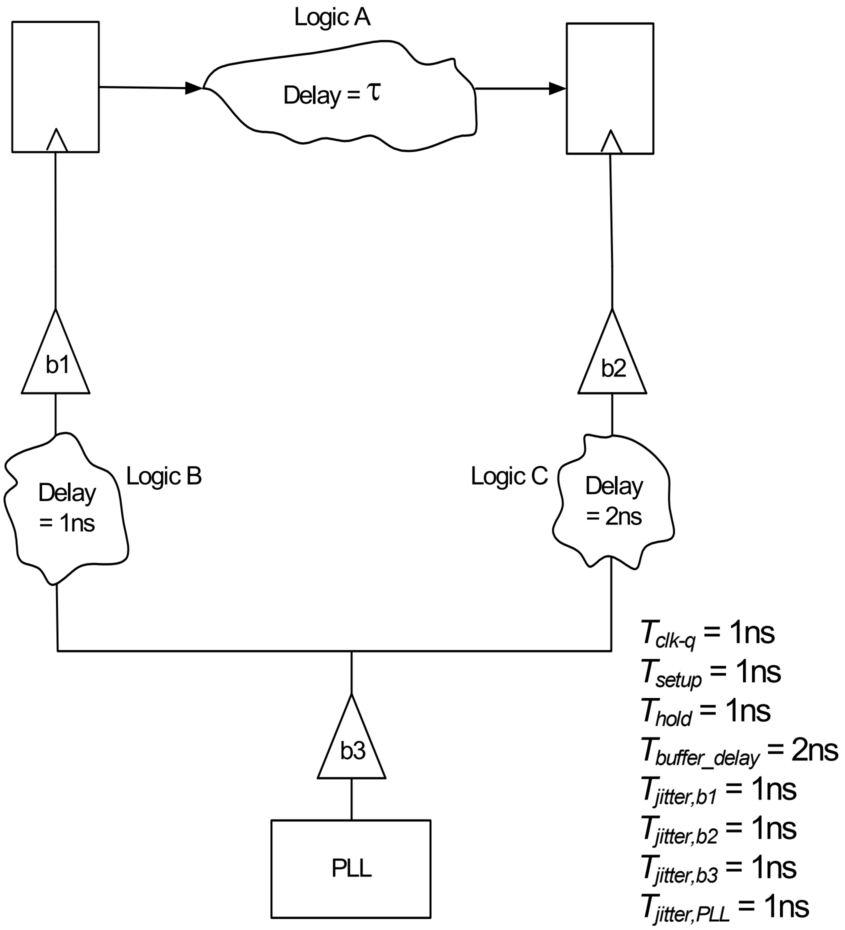
```
module test_question;
reg [3:0] c, d, e, f;

initial begin
   c = 3;
   #1 c = c + 1;
   d = c + 1;
   #1  //t = 2, question part (a)
   #1 e = 3;
   #1 e <= e + 1;
   f <= e + 1;
   #1  //t = 5, question part (b)
   end
endmodule
```

a) At time t = 2, what are the values of registers ‘c’ and ‘d’?

b) At time t = 5, what are the values of registers ‘e’ and ‘f’?

8.0 Problem 8 (17 Points) – Timing & Synchronization

The following circuit is operated with a clock period of 10ns.



$T_{clk\text{-}q} = 1\text{ns}$
$T_{setup} = 1\text{ns}$
$T_{hold} = 1\text{ns}$
$T_{buffer\_delay} = 2\text{ns}$
$T_{jitter,b1} = 1\text{ns}$
$T_{jitter,b2} = 1\text{ns}$
$T_{jitter,b3} = 1\text{ns}$
$T_{jitter,PLL} = 1\text{ns}$

Figure 8. Circuit for Problem 8.0.

a) **(4 Points)** Which of the circuit elements shown in the diagram could introduce *skew* and why?

b) **(6 Points)** Assume all delays are at their nominal values as shown. **Excluding jitter**, what is the *minimum* and *maximum* delay of **Logic A (i.e., what is τ)**? **Give both numerical solutions and equations, indicating clearly the source of each delay.** *Your answers should be in the form "* $x < \tau < y$ *".*

c) **(7 Points)** Repeat part (b), but now **include the effects of jitter**. Assume that the three buffers and the PLL can each introduce a maximum *cycle-to-cycle* jitter of 1ns, and that these values are uncorrelated. Clearly show and explain your equations. Again, clearly indicate the source of each delay. (For example, instead of generically writing T_{jitter}, write $T_{jitter}(b_x)$ to indicate a particular jitter term comes from buffer b_x).