EECS 452 *Midterm* Closed book part

Fall 2011

Name: ___________________________________ unique name: _______________

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

____

Scores:

#	Points
Closed book	
Page 2	/14
Page 3	/11
Open book	/ 75
Total	**/100**

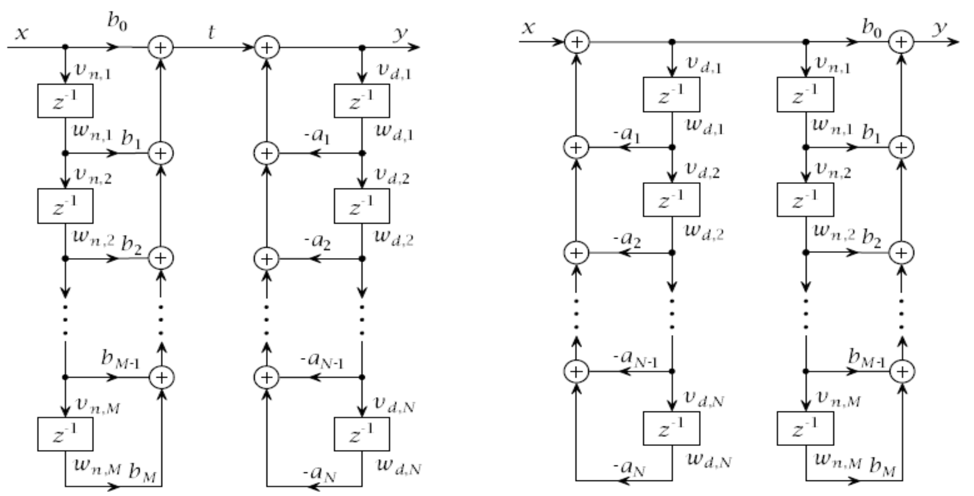
NOTES:

- There are **3** pages including this one.
- On the *closed book* section you may not have books, notes, but you *may* have a calculator. Nothing but a writing utensil and calculator is allowed.
- Don't spend too much time on any one problem.
- You have about 120 minutes for the exam. You probably shouldn't spend more than 25 on it

1. Say you take a 100-point DFT of the following signals with f_s= 500 Hz starting at time t=0. What would be what the non-zero DFT outputs would be (magnitude and phase)?
[4 each]
    a. $\sin(2\pi * 100t + \pi/2)$

    b. $3*\cos(2\pi * 20t + \pi/4) + 2$

2. When designing IIR filters we typically use cascaded biquad sections rather than (say) the form below.



    a. What is the potential problem with using the leftmost structure? **[2]**

    b. What is the potential problem with using the rightmost structure? **[2]**

    c. If breaking things into second order sections (biquads) is so useful, why don't we break them down further? **[2]**

3. *Fill in the blank or circle the correct answer*. Provide all numbers in decimal. **[11 points, -1 per wrong or blank answer, minimum 0]**

   a. An *anti-imaging filter* is always ***an FIR filter / an analog filter / found in front of a digital filter / used to address HSV issues in images***.

   b. For a given task you'd expect an ***FIR / IIR*** filter to have a higher order.

   c. A 4-bit 2's complement number can represent all integers from ____________ to ____________ (be exact).

   d. In the context of DSP, *MAC* stands for ***Machine Address Controller / Multiply And Accumulate / Mathematical Assembly and Control***.

   e. A 50Hz sine wave has a period of ____________________ μs.

   f. Say you have an ideal A to D converter which converts values from 4V to -4V to a 4-bit value. The worst-case quantization error is ±____________ Volts.

   g. In C, the *volatile* keyword indicates that ***the compiler should assume the value could change on its own / that the device could catch fire / that the code should be optimized for DSP applications.***

   h. An N-point implementation of the FFT algorithm discussed in class requires approximately ***N^2 operations / N*(N/2) operations / Nlog(N) operations / N operations.***

   i. A 4-bit Q3 number multiplied by a 4-bit Q3 number will result in an 8-bit Q______ representation. The result of this operation will be between the values _________ and _________ inclusive (be exact).

   j. In Verilog you would indicate a 4-bit binary number with a value of 0110 by writing:

      ____

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Scores:

#	Points
Open book	
1	/12
2	/10
3	/7
4	/8
5	/8
6	/15
7	/10
8	/5
Total	**/75**

NOTES:

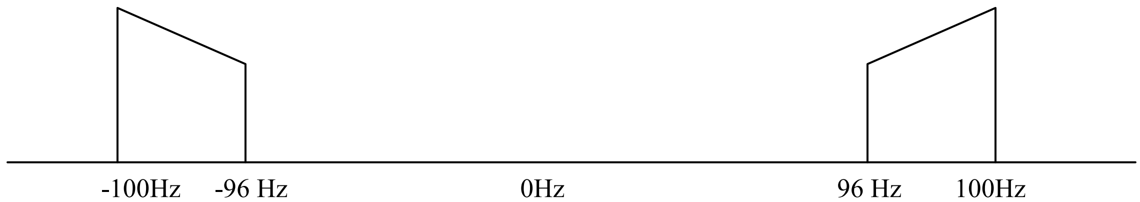
- There are **<u>9</u>** pages including this one.
- On the *open book* section you may use calculators, books and notes, but no PDAs, Portables, Cell phones, etc.
- Don't spend too much time on any one problem.
- You have about 120 minutes for the entire exam.
- Some questions may be much harder than others…

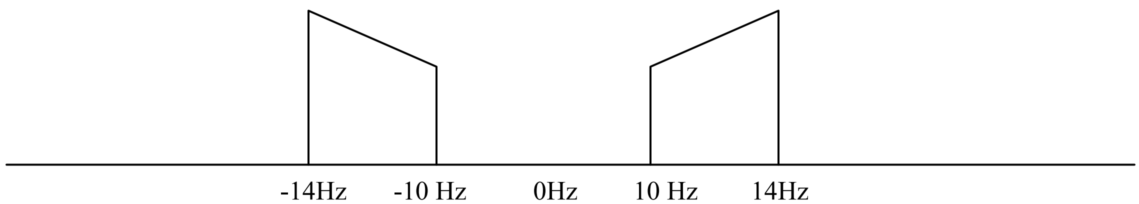
1) Consider the following transfer function:

a) Draw a block diagram that corresponds to that transfer function **[4]**

b) Indicate the range over a and b for which the filter <u>below</u> is stable. Your answer is to be should take the *format* of “$7<a<30$ and $-\infty<b\leq4$” or something similar. **[4]**

c) Assuming both a and b are both 0.5, *sketch* the pole/zero plot for the filter below. **[4]**





2) Aliasing can be used to frequency shift the spectrum of a band-limited waveform from higher to lower frequencies. For the spectra before sampling (top) and after (bottom) shown above, what is:
   a. The highest sampling rate (if any) that will yield the bottom spectrum? **[5]**

   b. The lowest sampling rate (if any) that will yield the bottom spectrum? (*Clearly* show your work.) **[5]**

3) You are given a stable digital filter described using a biquadratic transfer function of the form

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

and a sample rate of f_s Hz.

a) What is the value of H(z) at 0 Hz? **[3]**

b) If a_2=0.5, what is the largest (closest to positive infinity) that a_1 could be? Briefly justify your answer. **[4]**

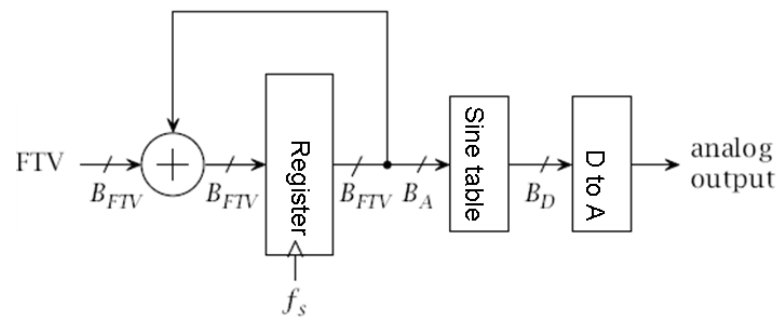
4) Spectral leakage
   a) What is the main cause of spectral leakage? **[2]**

   b) In lab we noticed that spectral leakage would vary over time (sometimes quite a bit) even though the input being sampled wasn't changing (it was a constant sine wave). Explain why that variance happened. **[3]**

   c) How did we reduce the spectral leakage variation in lab? **[3]**

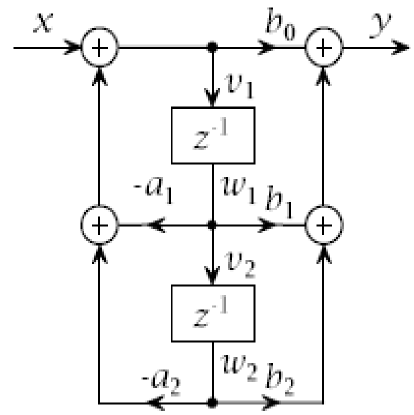
5) Say you are developing an application that needs to use Direct Digital Synthesis to generate sinusoids from 0 to 1000 Hz with frequency spacing in that range of no more than 2Hz. Assume that f_s=10000Hz.

   a) What is the minimum number of bits that must be kept in the "Register" (found in the figure below)? *Clearly* show your work or no credit will be given. **[4]**



   b) Given your answer above and assuming that the sine table must be a power of 2, what value should FTV be if you want to generate 447 Hz signal as closely as possible? Show your work. **[4]**

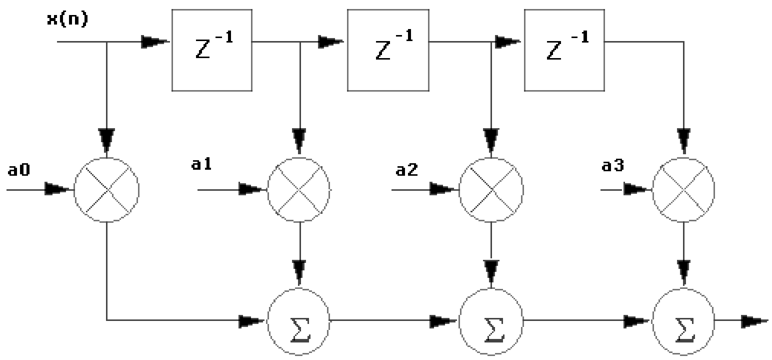
6) Write a C function with the following prototype:




```
Int16 cdf2 (Int16 b0, Int16 b1,
            Int16 b2, Int16 a1,
            Int16 a2, Int16 x,
            Int16 *w)
```

which implements the above transfer function (implementing it in the form given). All Int16s are to be in Q14 form.
[15 points]

7)



Consider a FIR filter above. Assume that:

- f_s=50KHz
- All coefficients are represented as 8-bit Q7 numbers
- The input and output are represented as 8-bit Q7 numbers.
- a0=0x40, a1=0x01, a2=0xff and a3=0xc0

a) How can you know that this filter has linear phase? **[2]**

b) Is the filter stable? How do you know? **[2]**

c) What is the group delay of this filter? **[2]**

d) Assuming a 100 Hz signal is in the passband for this filter, what is the phase of the output relative to a 100 Hz sine wave? **[2]**

e) What is the maximum value (closest to positive infinity) that this filter can output? Write as a decimal. **[2]**

8) What are the pros and cons of using an FPGA rather than a processor to implement a filter?
[5]