EECS 452 *Midterm* Closed book part

Fall 2011

Name: KEY unique name: Key.

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

____

Scores:

#	Points
Closed book	
Page 2	/14
Page 3	/11
Open book	/ 75
Total	**/100**

NOTES:

- There are **3** pages including this one.
- On the *closed book* section you may not have books, notes, but you *may* have a calculator. Nothing but a writing utensil and calculator is allowed.
- Don't spend too much time on any one problem.
- You have about 120 minutes for the exam. You probably shouldn't spend more than 25 on it

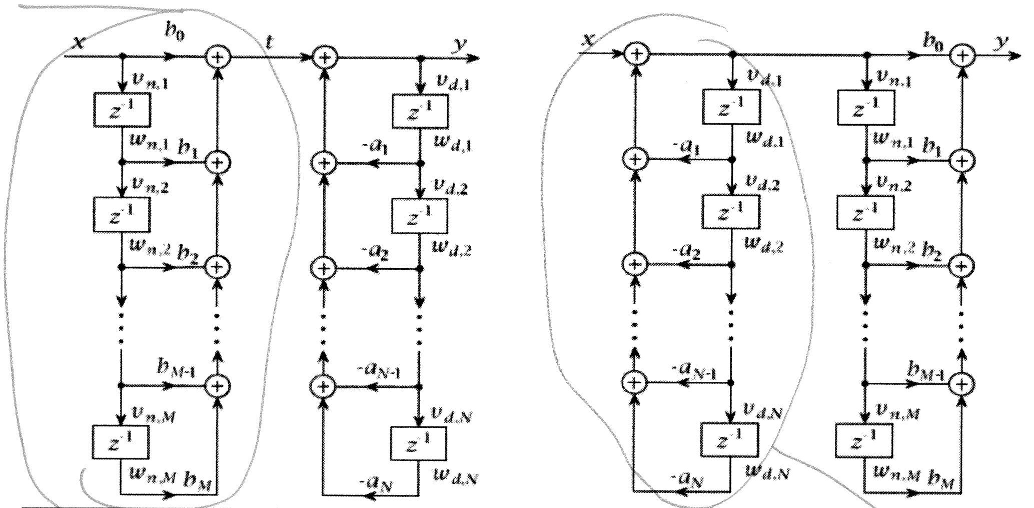
1. Say you take a 100-point DFT of the following signals with f_s= 500 Hz starting at time t=0. What would be what the non-zero DFT outputs would be (magnitude and phase)? **[4 each]**
   a. sin(2 π *100t+ π/2)

      $X(20) = 50 \angle 0$
      $X(80) = 50 \angle 0$

   b. 3*cos(2 π *20t+ π/4) + 2

      $X(4) = 150 \angle 45^\circ$
      $X(96) = 150 \angle -45^\circ$
      $X(0) = 200 \angle 0$

2. When designing IIR filters we typically use cascaded biquad sections rather than (say) the form below.



   a. What is the potential problem with using the leftmost structure? **[2]**

      The FIR side can underflow

   b. What is the potential problem with using the rightmost structure? **[2]**

      The feedback side (poles) can overflow.

   c. If breaking things into second order sections (biquads) is so useful, why don't we break them down further? **[2]**

      Doing so would create Complex Coef.

3. _Fill in the blank or circle the correct answer_. Provide all numbers in decimal. **[11 points, -1 per wrong or blank answer, minimum 0]**

   a. An *anti-imaging filter* is always ***an FIR filter / an analog filter / found in front of a digital filter / used to address HSV issues in images***.

   b. For a given task you'd expect an ***FIR / IIR*** filter to have a higher order.

   c. A 4-bit 2's complement number can represent all integers from ___-8___ to ___7___ (be exact).

   d. In the context of DSP, *MAC* stands for ***Machine Address Controller / Multiply And Accumulate / Mathematical Assembly and Control***.

   e. A 50Hz sine wave has a period of ___20,000___ μs.

   f. Say you have an ideal A to D converter which converts values from 4V to -4V to a 4-bit value. The worst-case quantization error is ±___1/4 .25___ Volts.

   (8V/16) 1/2

   g. In C, the *volatile* keyword indicates that ***the compiler should assume the value could change on its own / that the device could catch fire / that the code should be optimized for DSP applications.***

   h. An N-point implementation of the FFT algorithm discussed in class requires approximately ***N^2 operations / N*(N/2) operations / Nlog(N) operations / N operations.***

   i. A 4-bit Q3 number multiplied by a 4-bit Q3 number will result in an 8-bit Q___6___ representation. The result of this operation will be between the values ___1___ and ___-7/8 (-.875)___ inclusive (be exact).

   j. In Verilog you would indicate a 4-bit binary number with a value of 0110 by writing:
   ___4'b0110___

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Scores:

#	Points
Open book	
1	/12
2	/10
3	/7
4	/8
5	/8
6	/15
7	/10
8	/5
Total	**/75**

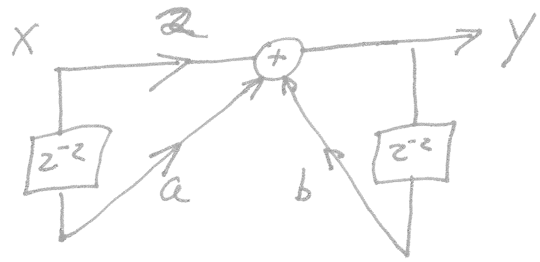
NOTES:

- There are **9** pages including this one.
- On the *open book* section you may use calculators, books and notes, but no PDAs, Portables, Cell phones, etc.
- Don't spend too much time on any one problem.
- You have about 120 minutes for the entire exam.
- Some questions may be much harder than others…

1) Consider the following transfer function:

$$H(z) = \frac{2 + a * z^{-2}}{1 + b * z^{-2}}$$

a) Draw a block diagram that corresponds to that transfer function **[4]**



b) Indicate the range over a and b for which the filter <u>below</u> is stable. Your answer is to be should take the *format* of "7<a<30 and -∞<b≤4" or something similar. **[4]**

$$H(z) = \frac{1 + a * z^{-2}}{1 + b * z^{-2}}$$

a any value

$-1 < b < 1$

if a=b also stable....

$-1 < b < 1$

$1 + b z^{-2} = 0$

$z^2 + b = 0$

$z^2 = -b$

$z = \pm\sqrt{-b}$

c) Assuming both a and b are both 0.5, *sketch* the pole/zero plot for the filter below. **[4]**

$$H(z) = \frac{2 + a * z^{-2}}{1 + b * z^{-2}}$$

zero

$2z^2 + .5 = 0$

$z^2 = -1/4$

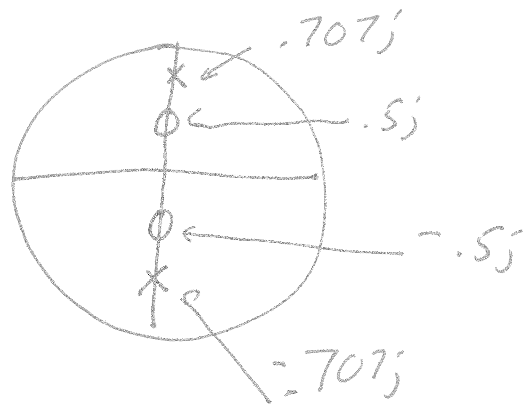
$z = \pm j\, 1/2$

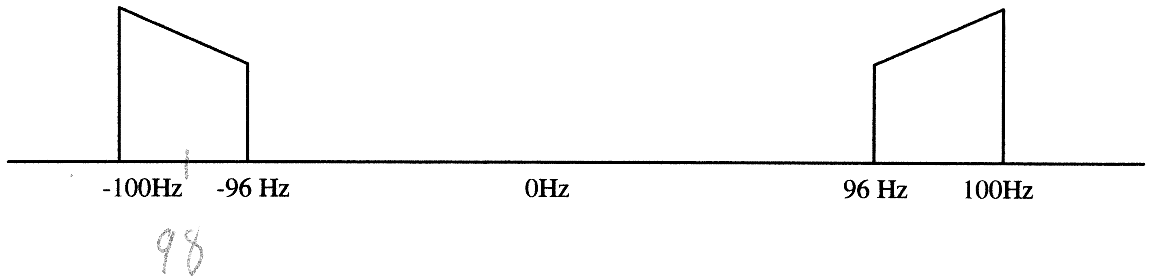
pole

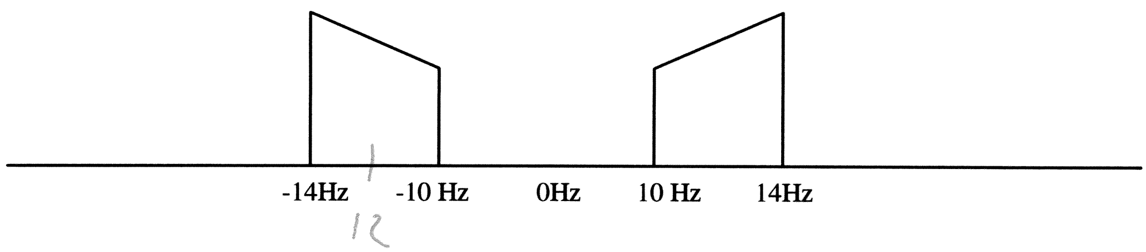
$z^2 + .5 = 0$

$z^2 = -1/2$

$z = \pm\sqrt{1/2} =$







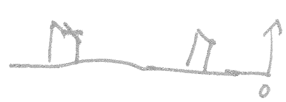
2) Aliasing can be used to frequency shift the spectrum of a band-limited waveform from higher to lower frequencies. For the spectra before sampling (top) and after (bottom) shown above, what is:

   a. The highest sampling rate (if any) that will yield the bottom spectrum? **[5]**

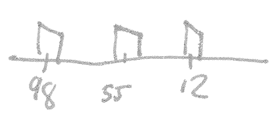
   $98_{Hz} - 12_{Hz} = 86$ Hz. Any thing larger shifts it farther.

   b. The lowest sampling rate (if any) that will yield the bottom spectrum? (*Clearly* show your work.) **[5]**

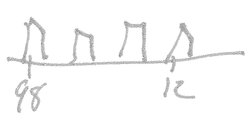
   must be > 28 Hz due to sampling theorem.

1 

= 86

2 

= 43

3 

$\boxed{28.\bar{6}}$ Hz

4 24.5 Hz too low

3) You are given a stable digital filter described using a biquadratic transfer function of the form

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}};$$

and a sample rate of f_s Hz.

a) What is the value of H(z) at 0 Hz? **[3]**

$$\frac{b_0 + b_1 + b_2}{1 + a_1 + a_2}$$

b) If a_2=0.5, what is the largest (closest to positive infinity) that a_1 could be? Briefly justify your answer. **[4]** Pretty tricky.

There are a lot of ways to do this.

$(z-p_1)(z-p_2) = z^2 - 2r\cos\theta z + r^2 = z^2 + a_1 z + a_2$

$1 + a_1 z^{-1} + a_2 z^{-2}$

$r^2 = .5, \quad r = \pm\sqrt{1/2}$

$z^2 + a_1 z + 0.5$

if $\theta = 0$, $2r = \sqrt{2}$.

$$\frac{-a_1 \pm \sqrt{a_1^2 - 2}}{2} = r_1, r_2$$

But this ignores real case.

$p_1 \cdot p_2 = 1/2$

$a_1^2 \geq 2$ roots are real

$|p_1| < 1$

$a_1 = \sqrt{2}$, roots are $\frac{-\sqrt{2}}{2}$

$|p_2| < 1$

$p_1 + p_2$?

$a_1 = 1.5$

$$\frac{-1.5 \pm \sqrt{(1.5)^2 - 2}}{2} \qquad \frac{-1.5 \pm .5}{2}$$

~~-2 to~~ -1 to -.5

worst case is one pole = .5, other 1.

$$\frac{-1.5 \pm \sqrt{.25}}{2}$$

1.5

1.5

4) Spectral leakage

a) What is the main cause of spectral leakage? **[2]**

Freq. components in sampled signal that do not exactly match a given bin in the DFT.

b) In lab we noticed that spectral leakage would vary over time (sometimes quite a bit) even though the input being sampled wasn't changing (it was a constant sine wave). Explain why that variance happened. **[3]**

~~The input pha~~

The phase of the input ~~[illegible]~~ changes over time.

That phase impacts ~~[illegible]~~ where the leakage shows up.

c) How did we reduce the spectral leakage variation in lab? **[3]**

Windowing

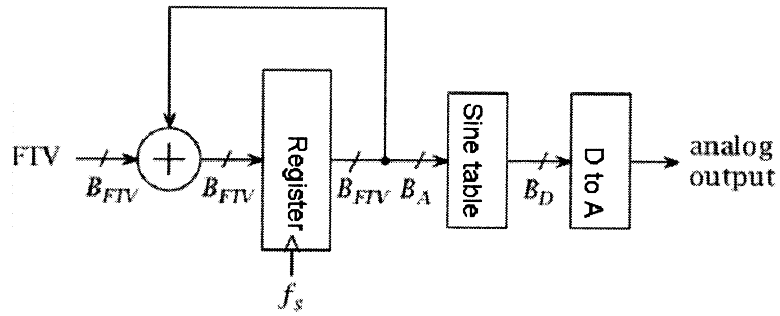
5) Say you are developing an application that needs to use Direct Digital Synthesis to generate sinusoids from 0 to 1000 Hz with frequency spacing in that range of no more than 2Hz. Assume that f_s=10000Hz.

a) What is the minimum number of bits that must be kept in the "Register" (found in the figure below)? *Clearly* show your work or no credit will be given. **[4]**

$\frac{10,000}{2} = 5000$

$2^{13} > 5000$

13 bits



b) Given your answer above and assuming that the sine table must be a power of 2, what value should FTV be if you want to generate 447 Hz signal as closely as possible? Show your work. **[4]**

$\frac{10,000}{2^{13}} X = 447$

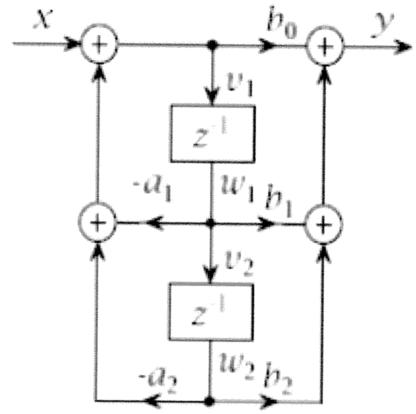
$\frac{447 \cdot 2^{13}}{10,000} = X$

$X = 366.1824$

366

6) Write a C function with the following prototype:

```
Int16 cdf2 (Int16 b0, Int16 b1,
            Int16 b2, Int16 a1,
            Int16 a2, Int16 x,
            Int16 *w)
```



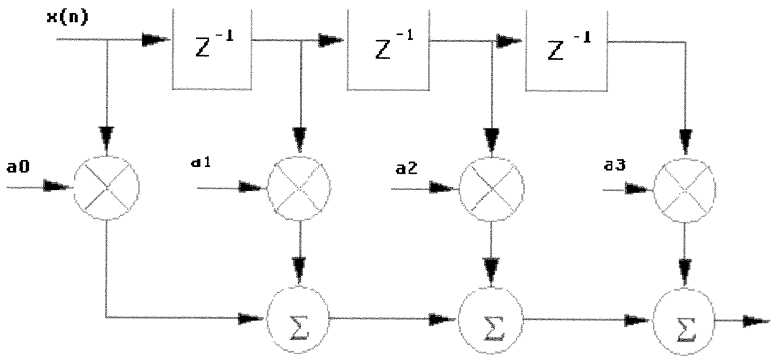
which implements the above transfer function (implementing it in the form given). All Int16s are to be in Q14 form.
[15 points]

```
Int16 cdf2 (Int16 b0, Int16 b1, Int16 b2, Int16 a1, Int16 a2,
            Int16 x, Int16 *w)
{
      long T,yQ29;
      int TQ15;

      T = ((long) x) << 14 - (long)w[0] * a1 - (long)w[1] * a2;
      TQ15 = (T + 1<<13) >> 14;
      yQ29 = (long) TQ14 * b0 + (long) w[0] * b1 + (long) w[1] * b2;
      w[1] = w[0];
      w[0] = TQ15;

      yQ29 = (yQ29 + 1<<13) >> 14;
      if (yQ29 > 32767)
            return 32767;
      if (yQ29 < -32768)
            return 32768;
      return yQ29;
}
```

7)



Consider a FIR filter above. Assume that:

- f_s=50KHz
- All coefficients are represented as 8-bit Q7 numbers
- The input and output are represented as 8-bit Q7 numbers.
- a0=0x40, a1=0x01, a2=0xff and a3=0xc0

a) How can you know that this filter has linear phase? **[2]**

The filter coefficients are anti-symmetric, i.e. a0 = -a3 and a1 = -a2.

b) Is the filter stable? How do you know? **[2]**

Yes. All FIR filters are stable. (It has no feedback loops. All the poles are at the origin and thus inside the unit circle.)

c) What is the group delay of this filter? **[2]**

(N-1)/2 = 1.5 samples or 0.03 ms

d) Assuming a 100 Hz signal is in the passband for this filter, what is the phase of the output relative to a 100 Hz sine wave? **[2]**

phase = 2*pi*f*(group delay) = 0.006pi

e) What is the maximum value (closest to positive infinity) that this filter can output? Write as a decimal. **[2]**

Sum of the absolute values of the coefficients is 65/64. But the largest value can be represented by 8-bit Q7 number is 127/128 = 0.992.

8) What are the pros and cons of using an FPGA rather than a processor to implement a filter? **[5]**

Pros:

- Highly parallel operation allows certain filter forms to be run *very* quickly (for example, a transposed DF2 IIR filter).

Cons:

- Hard to code/debug. Need to use an HDL (like Verilog) rather than C.
- Often doing more than just filtering and other things almost certainly easier on a processor.
- Typically takes more power and has a higher cost.