EECS 452 Midterm *Exam*

Winter 2012

Name: _____ unique name: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

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Scores:

#	Points
Section I	/40
Section II	/30
Section III	/30
Total	**/100**

NOTES:

- Open book, open notes.
- There are **8** pages including this one.
- Calculators are allowed, but no smart phones, laptops, or other wireless devices are allowed.
- You have 120 minutes for the exam.
- **Be sure to show work and explain what you've done when asked to do so.** You will not receive partial credit without showing work.
- In the context of the exam you are to assume all signed numbers are two's complement numbers.

Section I -- Short answer 40 points

1) A 8 bit binary adder adds two values 0xA5 and 0x64 allowing overflow without saturation. What is the result (in Hexadecimal and Decimal) of the addition in the accumulator of this adder if the two input values are **[4]**

	Hex	Decimal
a) Unsigned binary numbers:	_____	_____
b) 2's complement binary numbers:	_____	_____
c) Unsigned Q4 binary numbers:	_____	_____
d) Signed (2's complement) binary Q4 numbers	_____	_____

2) Express the signed decimal fraction -0.625 in the following (Hex or binary) format **[2]**

a) 8 bit two's complement Q7: _____

b) 8 bit two's complement Q3: _____

3) The result of multiplying two 16 bit two's complement Q15 numbers together is a (put a check on the line next to the correct answer) **[4]**

a) 16 bit Q15 number: _____

b) 32 bit Q30 number: _____

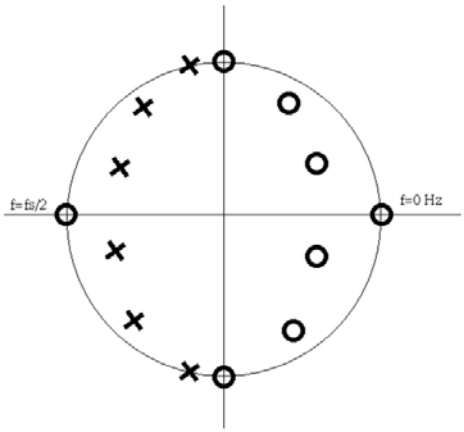
c) 32 bit Q15 number: _____

d) None of the above: _____

4) A 16 bit quantizer achieves a post-quantization SNR of 60dB. If you only needed attain a specification (spec) of 30dB post-quantization SNR could you reduce the number of bits in the quantizer to12 bits and still statisfy the spec? Why or why not? **[6]**

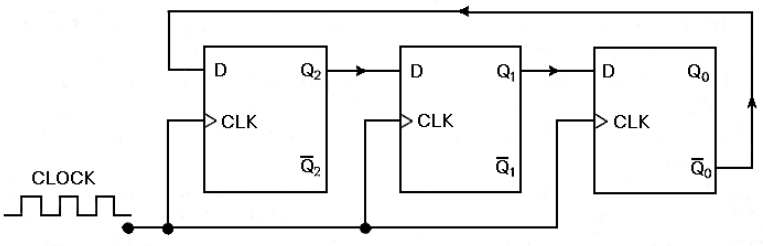
5) A digital spectrum analyzer of a continuous time signal uses discrete sampling and a 512 point FFT. If the frequency spacing in the FFT spectrum is to be at most 100Hz what is the maximum sampling frequency that the analyzer can handle? **[6]**

6) A certain filter has the pole zero constellation shown below. Is this an FIR or an IIR filter? What is the filter order? Is is lowpass, highpass, bandpass, or none of the above? **[6]**



7) The ADC of a DSP system samples an input signal at 48,000 samples/sec sampling rate. The signal is processed by dropping every even sample and sending only the odd samples to the DAC. Assume that the DAC inserts 1/24 msecs between each sample. If the input were a sinusoid at frequency 8kHz what would be the output of the DAC assuming no quantization error and an ideal reconstruction filter? **[6]**

8) The counter below uses 3 D flip flops. Draw the timing table indicating the states of the counter over the first 8 clock cycles (assume initial state is 000). What are the signal activity levels (α_1, α_2 and α_3) at the outputs Q2, Q1, Q0 of the counter? What is the total power dissipation of the counter assuming that the logic voltage is V_d=5V, the clock rate is f_{clk}=1MHz and the outputs of each flip flop see the same capacitance C=10pF? **[6]**



Section II – longer answers 30 points

1) You wish to implement a filter on a 16 bit DSP chip that runs at 250MHz to do audio signal filtering. On this DSP chip the number of clock cycles required for a complex vector multiply of two 128-element vectors is 1500 cycles. The number of cycles for a 128 point complex FFT or IFFT (with scaling) is 2500 cycles. The number of cycles required for computing the output of a 16^{th} order IIR filter is 1000 cycles [10].

   a) One implementation of the filter is to use a 16^{th} order IIR filter whose transfer function approximates the desired transfer function in both phase and magnitude. How many words of memory (16 bit words) are required to store the coefficients and the filter states in order implement this filter? What is the maximum sampling rate F_s such that the filter computation can be performed in real time, i.e. that the computation for the previous sample is completed before the next sample comes in? [4]

   b) Another implementation of the filter is to use a DFT filter bank that works as follows. Perform a 128 point FFT on the 128 previous input samples. Then multiply these complex values by the desired transfer function. Finally, perform the IFFT on the result. How much memory is required to store the coefficients and the filter states in order implement this filter? What is the maximum sampling frequency that can be used so that the filter computation can be performed in real time, i.e., so that the filter output can be computed on the previous 128 block of samples before the next sample comes in? [4]

   c) If you had a fast enough clock rate to handle all the computations in real time and enough memory storage capacity, are there any advantages to using the DFT filterbank as compared to the IIR filter? [2]

2) Consider the discrete time signal $x[n]=0.5*\cos(2\pi f_1 n)+\sin(2\pi f_2 n)$, $n=1,\ldots,8$. [10]

   a) What is the DFT of x[n] if $f_1=1/4$ and $f_2=3/8$? Carefully plot the magnitude and phase being sure to label and quantify the ranges of the axes. [5]
   b) If x[n] corresponded to a continuous-time signal x(t) sampled at 48kHz what frequencies (Hz) are present in the original signal x(t)? [3]
   c) Is there spectral leakage in this example? Why or why not? [2]

3) The input output relation of a particular linear time invariant digital filter is: [10]

$$y[n] = \sum_{k=0}^{N} (-1)^k x[n-k]$$

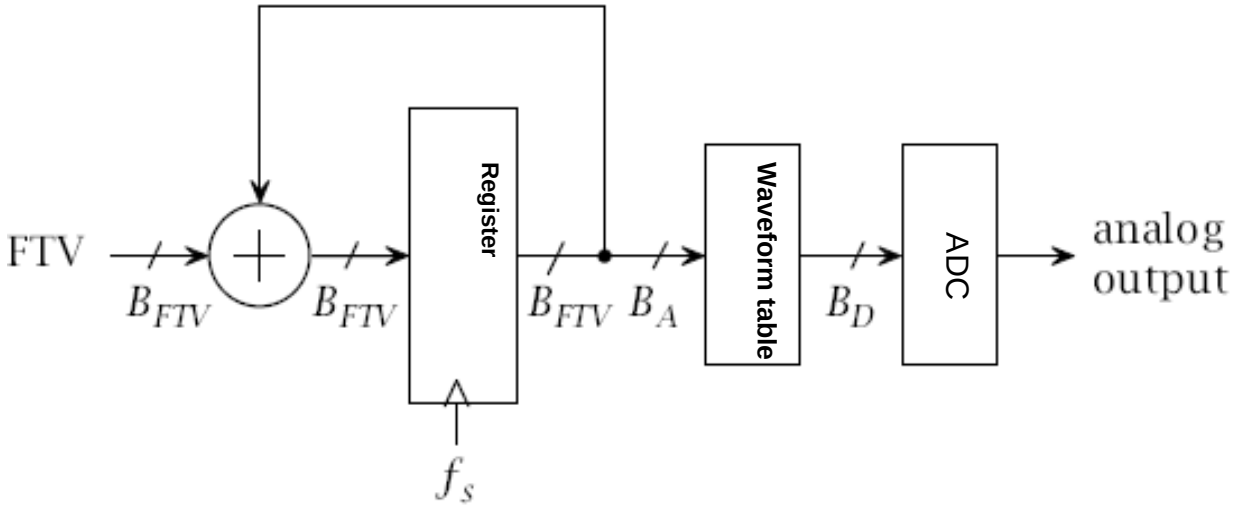
a) What is the transfer function H(z) associated with the filter? Plot poles-zeros constellation of H(z) in the complex plane. [3]

b) Compute and plot the magnitude and phase frequency response as a function of the digital frequency variable f of the DTFT. [3]

c) Is this filter linear phase? What is its group delay? [2]

d) Is this filter LP, BP, HP or none of the above? [2]

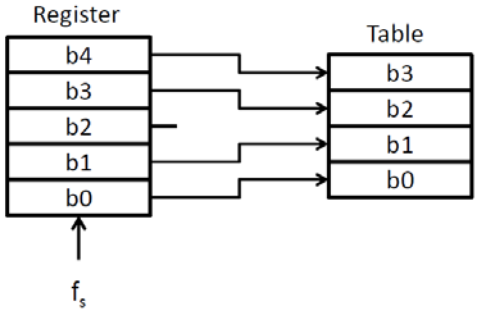
Section III Longer answers 30 points



1) A waveform synthesizer uses the DDS system above to generate a periodic waveform using a 4 bit waveform table containing 16 samples of a single period of the linear ramp waveform s[n]=n, n=0,1,2 … 15. **[15]**

   a) Assume FTV=1 and $B_A = B_{FTV}$. What should the clock frequency f_s (Hz) be in order for the output waveform frequency to be equal to 10kHz? Plot three or four periods of the analog output over time. Be careful to label your axes and indicate the amplitude and period of the waveform on your plot.**[7]**

   b) Now we modify the DDS by increasing B_{FTV} and connected the table and to the register in the following non-standard manner. We set $B_{FTV}=B_A+1$ and make the upper 2 MSB's of the register address the 2 MSB's of the waveform table and the lower 2 LSB's of the register address the 2 LSB's of the waveform table (see diagram below). What is now the output waveform frequency in terms of the clock rate f_s (Hz), B_{FTV} and B_A? What should the clock frequency be for the waveform frequency to be 10kHz? Plot a single period of the output assuming the linear ramp waveform you assumed in part a). **[8]**



2) Consider the digital filter below that produces an output y[n] given input x[n]. **[15]**

a) Is this filter FIR or IIR? What is the filter order? **[5]**

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b) Assuming that that the input is scaled appropriately is this filter implementable in 16 bit Q(14) arithmetic? Could it be implemented in 16 bit Q(15) with a small modification? If so how would you modify it? **[5]**

c) Can this filter be implemented with biquads as in Lab 5? How many biquads would be necessary? **[5]**