

EECS 452 *Midterm* Closed book part

Winter 2013

Name: _____ unique name: _____

Sign the honor code:

I have neither given nor received aid on this exam nor observed anyone else doing so.

Scores:

#	Points
Closed book	
Page 2	/17
Page 3	/10
Open book	/73
Total	/100

NOTES:

- There are **3** pages including this one.
- On the *closed book* section you may **not** have books, notes, or calculator. Nothing but a writing utensil.
- Don't spend too much time on any one problem.
- You have about 120 minutes for the exam. You probably shouldn't spend much more than 20 minutes on this section.

Closed book portion

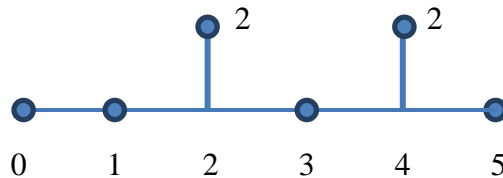
1. Say you took a 16-point DFT of the following signals with $f_s=3.2$ KHz starting at time $t=0$. What would the non-zero DFT outputs be (magnitude and phase)?

[3 points each]

a. $2 \cdot \sin(2 \pi \cdot 400t + \pi/2)$

b. $2 \cdot \cos(2 \pi \cdot 800t) - 2$

2. An FIR filter has the impulse response shown below. Assume $f_s=1$ ms. **[2 points each]**



- a. What is the difference equation for this filter?

- b. What is the transfer function for this filter?

- c. Is this filter linear? If so, what is the group delay? If not, why not?

3. Write a legal C function named “mult16” which takes two 16-bit Q15 numbers as arguments and returns their product as a 16-bit Q15 rounding appropriately. Use “short” as a 16-bit signed data type. **[5 points]**

4. *Fill in the blank or circle the best answer.* Provide all numbers in decimal.
[10 points, -1 per wrong or blank answer, minimum 0]
- If we multiply an 8-bit Q_6 value by an 8-bit Q_6 value the result would be a _____-bit Q _____ number.
 - _____ is the smallest number (closest to negative infinity) that can be exactly represented by a signed 11-bit Q_8 number. _____ is the largest number (closest to positive infinity) that can be exactly represented by a signed 5-bit Q_3 number.
 - In signed 5-bit two's complement Q_3 , what is the value of 10010? _____.
 - We say a filter has *linear phase* if the group delay is *independent of the input frequency / proportional to the input frequency / greater than the input frequency.*
 - Say you have an ideal A to D converter which converts values from 4V to -4V to a 5-bit value. In the ideal case, the worst-case quantization error is \pm _____ Volts.
 - One advantage of IIR filters compared to FIR filters is that IIR filters tend to *use fewer total components to implement the same functionality / be easier to make linear phase / be easier to make stable.*
 - FIR filters *can easily / cannot / can with great difficulty* implement a typical RC analog filter.
 - Most computers don't have a MAC instruction because
 - *it would likely cause the clock period to get longer.*
 - *they don't have an accumulator.*
 - *it interferes with floating point support.*
 - DSPs, on the other hand, do tend to have a MAC instruction because
 - *they generally do have an accumulator.*
 - *they commonly can take advantage of MAC instructions.*
 - *they don't generally have floating point instructions.*
 - *they have a very slow clock period to begin with.*
 - An N -point implementation of the FFT algorithm discussed in class requires approximately $N^2 / N^{1.5} / N \cdot \log(N) / N$ operations.
 - A waveform is sampled using a sample rate of 42 KHz. If you desire a frequency spacing of 2 Hz in the DFT of the sample set, you'll need to sample for _____ ms.

EECS 452 *Midterm* Open book part

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Scores:

#	Points
Open book	
Page 2	/11
Page 3	/11
Page 4	/12
Page 5	/15
Page 6	/11
Page 7	/13
Total	/73

NOTES:

- There are **7** pages including this one.
- On the *open book* section you may use calculators, books and notes, but no PDAs, Portables, Cell phones, etc.
- Don't spend too much time on any one problem.
- You have about 120 minutes for the entire exam.
- Some questions are much harder than others...
- ***When asked to show your work do so. If the question asks you to show your work and you don't you will get no points, even if the answer is correct.***
- If you need to use the back of the exam paper for your answers, you must make it clear that the grader is to look there.

Short answer:

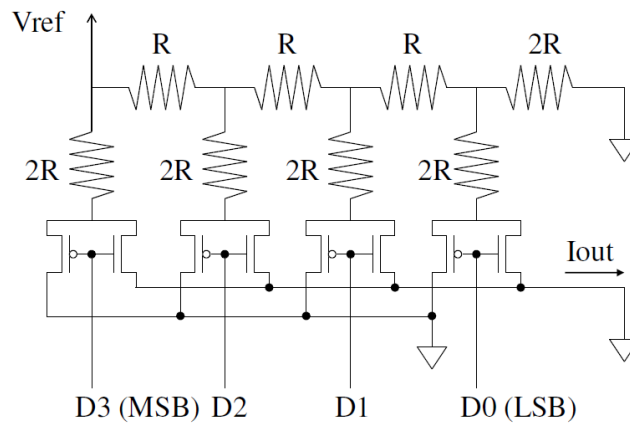
1. Say you took a 32-point DFT of the following signals with $f_s=1.6$ KHz starting at time $t=0$. What would be what the non-zero DFT outputs would be (magnitude and phase)? Briefly justify your answers.

[6 points, 3 points each]

- $2 \cdot \sin(2 \pi \cdot 1000t)$

- $2 \cdot \cos(2 \pi \cdot 1600t - \pi/8)$

2. Answer the following questions about the ideal digital-to-analog converter shown below. **[5 points]**



a. Assuming $V_{ref}=12V$ and $R=1k\Omega$, if $D[3:0]=1001$, what is I_{out} ? **[3]**

b. If we were going to make a 12-bit converter using this R/2R ladder scheme, how many resistors would we need? **[2]**

3. Say you are building an FIR bandpass filter that will have a passband of 1KHz centered at 8KHz. Further, say that there is a fair bit of signal in the input up to 40KHz.

[8 points]

- Without an anti-aliasing filter, what is the lowest frequency you could sample the data? **[3]**

- What would happen if you sampled at a lower frequency than that? **[2]**

- If you do have a (low-pass) anti-aliasing filter which has a passband that ends at 10KHz and a stopband that starts at 20KHz, what is the lowest frequency you could sample the data? You are to assume the gain of the anti-aliasing filter is 1.0 in the passband, 0 in the stopband, and unknown otherwise. **[3]**

4. Draw a block diagram which corresponds to the following difference equation. **[3 points]**

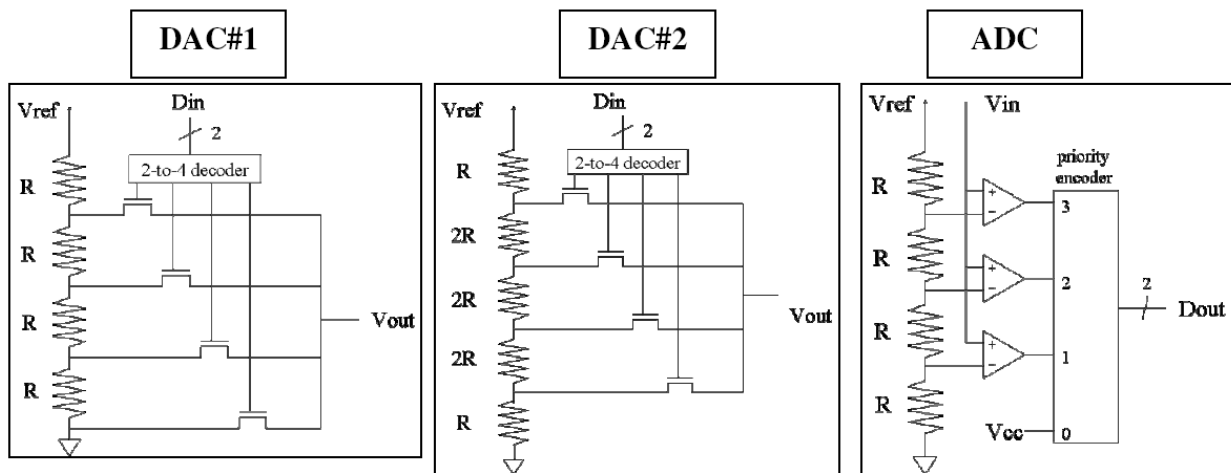
$$y[n] = x[n-1] + x[n-3] - y[n-2]$$

5. Consider the following difference equation [6 points]

$$y[n] = x[n] + 0.2 * x[n-2] + 0.4 * y[n-2]$$

- Write the transfer function which corresponds to that difference equation. [3]

- Is that filter stable? Show your work. [3]



6. Answer the following question using the above figures. Assume $V_{ref}=4V$ and that all converters are ideal. [6 points]

- If 2.4V is put into the ADC and D_{out} is connected to D_{in} of DAC#1, what is the value found on V_{out} of DAC#1? [2]

- If 2.4V is put into the ADC and D_{out} is connected to D_{in} of DAC#2, what is the value found on V_{out} of DAC#2? [2]

- If D_{in} of DAC#2 is "01" and the output of that DAC is connected to the V_{in} of the ADC, what is the output of the ADC? [2]

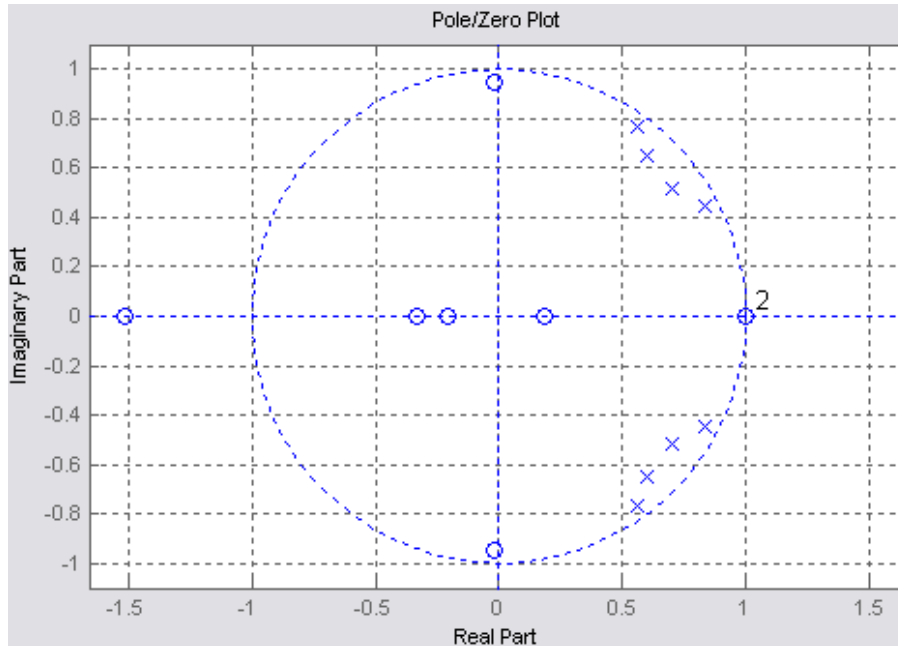
Longer answer

7. Consider the following filter transfer function:

$$H(z) = 0.25 * z^{-1} - 0.5 * z^{-3}$$

Write a function, `int trans(int x, int *w)` which takes a single input `x`, and returns the output of the filter. You may assume that the array `w` is of any fixed size you find useful. All inputs are in 32-bit Q31 and the output is also to be in 32-bit Q31. If the output is determined to be outside of the range of a 32-bit Q31 you should saturate. You are to write this for a machine where an `int` is 32 bits and a `long` is 64 bits. This function will be called iteratively with a new value of `x` passed in each cycle but with a pointer always to the same `w`, so your code needs to update `w` appropriately in addition to returning the output value. **[15 points]**

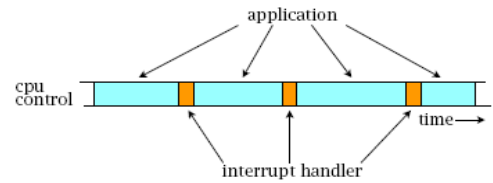
8. Consider the following pole/zero plot [11 points]



a) What type of filter (lowpass, highpass, bandpass, bandstop) is this? [2]

b) Draw a rough sketch of the frequency response of this filter. [3]

c) Circle the pole-zero combination that you would use for each biquad section to minimize the likelihood of overflow in your fixed-point implementation. Label each combination (1, 2, etc.) corresponding to the order you would cascade the biquad sections (the biquad section closest to the input being 1, the next 2, etc.) [6]



9. FFTs in the real world: [13 points]

On this question we will explore an FFT implementation on a processor and explore the impact interrupts have on our ability to do DSP work. For this entire problem, assume the following:

- An N -point implementation of the FFT requires $N/2 \log N$ complex arithmetic operations, where N must be a power of 2.
- Each complex arithmetic operation consumes 5 clock cycles on a CPU with a clock frequency of 100MHz.
- We are sampling audio data at a rate of 50 kHz.
- Our application requires us to not miss any of our samples.

a) Say we've written our program such that we grab X samples from our ADC as they come in and then after the last has arrived we need to start and complete our computation of the FFT over those X samples before the next sample arrives. (So we can do real-time spectrum analysis.) What is the largest FFT we'll be able to compute (that is, the largest value of X)? What will be the frequency resolution of that FFT? Clearly show your work! [5]

b) Now let us assume that:

- We have a timer that interrupts our processor at a rate of 50 kHz and that that interrupt routine grabs a sample for us.
- The interrupt routine takes 50 cycles to run.

i) If we want to do real-time spectrum analysis, what is the largest FFT would be able to compute? Don't worry if your answer seems unrealistic. Clearly show your work. [4]

ii) If all other assumptions remain the same, what is the slowest clock frequency the processor could have and still be able to do a 1024 point FFT in real-time? Clearly show your work! [4]