

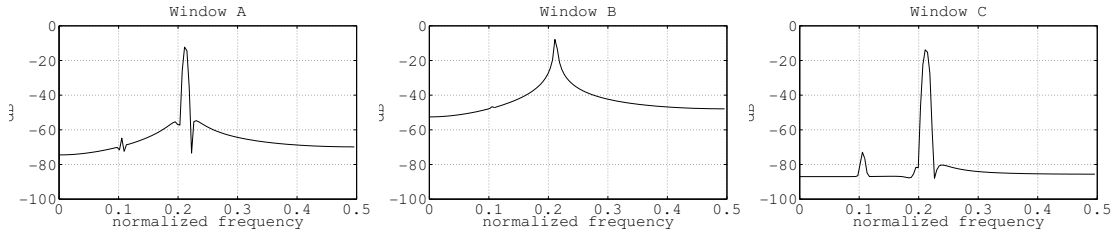
Part I: fill in the blanks (20 points)

1. (20 pts total, 1 pt per blank) Fill in the blanks.

- (a) A B-bit two's complement Q(B-2) number can represent all numbers from -2 to $2 - 2^{-(B-2)}$.
- (b) What needs to be placed between the carry in and the carry out of a one-bit adder to make it into a bit-serial adder?
A stage of delay (register, latch, etc.)
- (c) The 6-bit two's complement Q3 number 110101 is -1.375 in decimal.
- (d) What is unsigned binary 1111001000110111 in hex? (F237)_h.
- (e) Two's complement multiplication of 1110 and 1010 gives: 00001100.
- (f) If we multiply a 16-bit Q6 value by a 14-bit Q5 value the result is a 30-bit Q 11 value.
- (g) A 5-bit A/D converter has 32 levels/bins. If the input magnitude ranges from -2 to 2 V, and use two's complement 5-bit Q_x to represent the output, what is the most natural choice of x : Q3. The absolute error of this ADC is at most 0.0625 V.
- (h) A bandpass signal with frequency component limited to the range $[44, 46]$ MHz is sampled at frequency F_s . Please indicate where the frequency component appears on the spectrum between $[-F_s/2, F_s/2]$.
- (1) $F_s = 45$ MHz: $[-1, 1]$ MHz.
- (2) $F_s = 16$ MHz: $[-4, -2]$ MHz.
- (i) In order to have a frequency spacing of 2 Hz in a 1024-point DFT, you should sample at a rate of 2048 Hz.
- (j) An averaging filter with order 10 has a constant group delay of (please fill in both the number and its unit) 5 sample times.
- (k) The filter preceding an A/D converter is called anti-aliasing filter.
- (l) The filter following a D/A converter is called anti-imaging filter.
- (m) An N -point implementation of the Radix-2 FFT algorithm discussed in class requires approximately $N \log N$ operations.
- (n) In IIR filter design when matching poles and zeros, we start with the pole closest to the unit circle, and match it with a zero that is the closest to it.

Part II: short questions (50 points)

2. (6 pts) We introduced three window functions to reduce leakage. The figure below shows the effects that each window has on the same data set. Please provide the name of the window in each case.



- (a) (2 pts) Window A:

Solution: *Hamming*

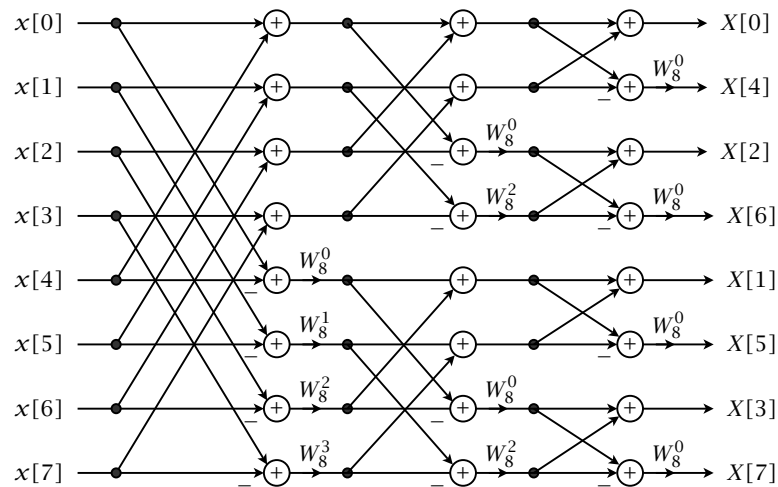
- (b) (2 pts) Window B:

Solution: *Rectangle*

- (c) (2 pts) Window C:

Solution: *Chebyshev*

3. (2 pts) What computational process does the following diagram illustrate? The answer does not have to be long (1-2 lines), but please be as specific as possible.



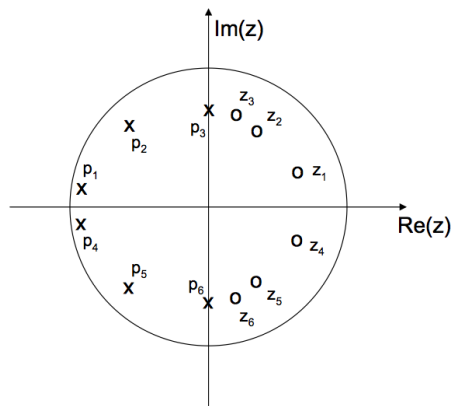
Solution: *This an 8-bit FFT done with decimation-in-frequency (DIF).*

4. (6 pts; 2pts each) Please find the group delay for the following FIR filters (unspecified coefficients in each case are assumed to be zero), assuming a sampling rate of $F_s = 1\text{KHz}$:

- (a) $h[0] = 0.875, h[1] = -0.5, h[2] = 0.875$.
- (b) $h[0] = 0, h[1] = 0.875, h[2] = -0.5, h[3] = 0.875$.
- (c) $h[0] = -0.5, h[1] = 0.875, h[2] = 0.875, h[3] = -0.5$.

Solution: The group delays are $2/2 = 1$, $4/2 = 2$, and $3/2 = 1.5$ sample times, respectively, or 1ms , 2ms , and 1.5ms , respectively.

5. (6 pts) The figure below shows the pole-zero locations of a filter.

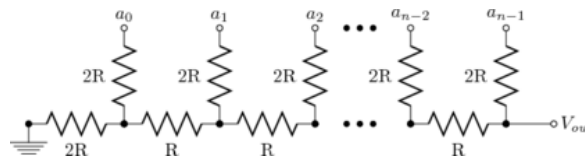


- (a) (3 pts) Illustrate how you would organize the poles and zeros into bi-quad sections, using the labels given in the figure.
- (b) (1 pt) Which biquad has the highest internal input to section output gain?
- (c) (2 pts) Sketch the filter transfer function $|H(f)|$, assuming a sampling rate of 48KHz , and classify this filter as lowpass, highpass, bandpass, bandstop, or none of the above.

Solution: Biquad 1 pairs $(p3, p6)$ with $(z1, z4)$; biquad 2 pairs $(p2, p5)$ with $(z2, z5)$; biquad 3 pairs $(p1, p4)$ with $(z3, z6)$.

This is a highpass filter with the passband starting at 12KHz .

6. (3 pts) Consider the following circuits.

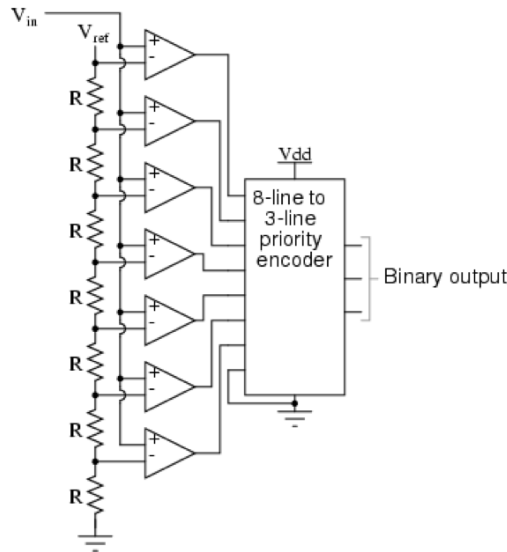


(a) (1 pt) What is the purpose of this circuit? **Solution:** *This is an n-bit R-2R ladder DAC.*

(b) (2 pts) Assume a bit a_i is attached to $V_{ref} = 12V$ if its value is 1 and grounded if its value is 0. Take $n = 8$. If the bits are (from MSB to LSB) 10101001, what is V_{out} ?

Solution: V_{out} is $10101001_b \times \frac{1}{2^8} \times V_{ref} = \frac{169 \times 12}{256} = 7.92V$.

7. (3 pts) Consider the following circuit:



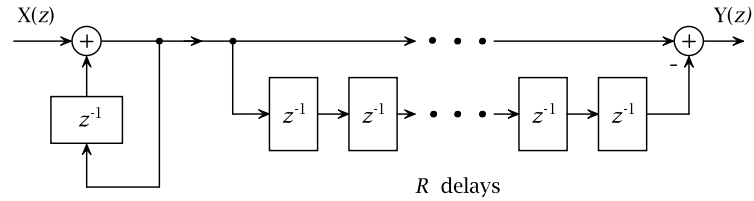
(a) (1 pt) What is the purpose of this circuit?

Solution: *This is an 8-bit flash ADC.*

(b) (2 pts) For $V_{in} = 0.56V_{ref}$ and $V_{in} = 0.79V_{ref}$, what are the corresponding output?

Solution: *The outputs are 100 and 110, respectively, corresponding to the 4th and the 6th bins.*

8. (6 pts) Consider the filter shown below.



(a) (2 pts) What is the transfer function of this filter? (show your work)

Solution: We can break the unit into the cascade of two systems. Let the first have output Y_1 . For the first delay stage we have its $Y_1 = X + z^{-1}Y_1$ giving

$$\frac{Y_1}{X} = \frac{1}{1 - z^{-1}}$$

The transfer function of the second part is trivially $1 - z^{-R}$. The composite transfer function is the product of the two individual transfer functions:

$$\frac{Y}{X} = \frac{1 - z^{-R}}{1 - z^{-1}}$$

(b) (1 pt) Of what type is this filter (FIR or IIR)?

Solution: FIR; or averaging filter

(c) (1 pt) What is the order of this filter?

Solution: $R - 1$

(d) (2 pts) Does this filter have constant group delay? If not why? If so what is the group delay in seconds for $R = 11$ and a sample rate of 100KHz?

Solution: Yes it does, because all its coefficients are equal. R is the order of the filter. Using known results on linear phase FIR filters, the group delay of the filter is $10/2$ samples. This gives a group delay of $\frac{R-1}{2} \cdot \frac{1}{100000} = 0.05$ ms.

9. (5 pts) We are implementing an FIR filter on a processor with a CPU clock of 500MHz. Assume that the number of CPU cycles required to compute an output sample = $a \times \text{Number of filter taps} + b$, where a and b are constants. We have measured the number of cycles required for a 200 tap and a 500 tap FIR filter to be 2450 and 6050 cycles, respectively.

(a) (3 pts) What are the values of a and b ?

(b) (2 pts) If we have a sampling rate of 40KHz, what is the largest filter that we can use on this processor?

Solution:

(a)

$$a = \frac{(6050 - 2450)}{(500 - 200)} = 12, \quad b = 2450 - 12 \times 200 = 50$$

(b) *The maximum number of CPU clocks we can afford for our filter is $500\text{MHz}/40\text{kHz}=12500$ cycles. This would give us enough time to compute the output of the filter to the current sample, before the next sample arrives. Plugging this number into the equation above, we can compute the maximum number of taps.*

$$\text{Number of Taps} = (12500 - 50)/12 = 1037$$

10. (7 pts) Consider two variables x, y (Int16 x, y); x is 16-bit Q15 and y is 16-bit Q14, both in two's complement format.

- (a) (3 pts) Multiply x by y , and convert the result back to a two's complement 16-bit Q15 number and store it a variable called `res`. Write two lines of C code that achieve this (including rounding).
- (b) (2 pts) Suppose $x = 0x6000$ and $y = 0x6000$. What is `res` in two's complement and in decimal?
- (c) (2 pt) What do you get when you do multiplication $x \times y$ in decimal? Is this the same as the value of `res`? If not, why?

Solution:

(a) *Since x and y are 16-bit variables, their product is 32-bits and it has $15+14=29$ fractional bits. It follows that we have*

```
Int32 temp = (Int32)x * (Int32)y;
Int16 res = Int16( (temp + 0x2000) » 14 );
```

(b) *We have $x \times y = 0x\ 24000000$, which means $res=(Int16)(0x24002000 \gg 14) = (Int16)\ 0x9000 = -28672$. Thus in decimal $res=(-28672)/2^{15} = -0.875$*

(c) *x corresponds to $24576/2^{15} = 0.75$ and y corresponds to $24576/2^{14} = 1.5$. Clearly an overflow has occurred here. In other words $0.75 \times 1.5 = 1.125$, but res is a 16-bit Q15 number and its range is from -1 to 1, so the results cannot fit in this number.*

11. (6 pts) Consider the signal $s(t) = \cos(2\pi(3000)t) + \sin(2\pi(4000)t + \frac{3\pi}{4})$.

(a) (1 pt) What is the smallest sampling frequency to use in order to avoid aliasing?

Solution: $f_s = 8\text{KHz}$

(b) (1 pt) Suppose we sample the signal at the rate you decided in (a), how many samples do we need in order to have a frequency spacing of 2Hz in the DFT?

Solution: $N = 4\text{K samples}$

(c) (1 pt) If we sample the signal at rate $f_s = 16\text{KHz}$ followed by DFT, what is the smallest number of samples required in the DFT to avoid aliasing and leakage?

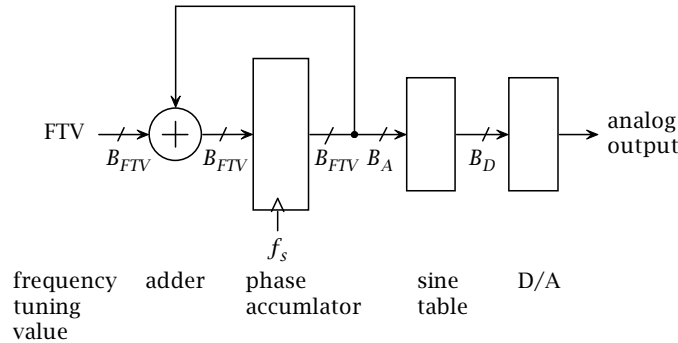
Solution: $N = 16$

(d) (3 pts) What is the DFT output using your choice in (c)?

Solution: *We have $X[3] = 8\angle 0$, $X[4] = 8\angle \frac{\pi}{4}$, $X[13] = 8\angle 0$, $X[12] = 8\angle -\frac{\pi}{4}$*

Part III: longer questions (30 points)

12. (12 pts) Consider the DDS diagram shown below.



You are asked to use the DDS shown above to generate sine wave output with a frequency of $F_o = 300\text{Hz}$ and an amplitude range $[-1, 1]$ Volt. In addition, (1) the generated sine wave cannot have more than 4mV error due to time quantization, i.e., you need to have a sufficient number of samples within each sine period so that the difference between two successive samples is no more than 4mV ; (2) the error due to amplitude quantization introduced by the DAC is no more than 2mV (i.e., the values before and after the ADC should not differ by more than 2mV). You may use the relationship $|\sin(a) - \sin(b)| < |a - b|$ to simplify your computation. Assume clock rate $f_s = 10\text{MHz}$. To satisfy all the above requirements:

- (a) (4 pts) How many entries do you need to keep in the sine table, and what should your choice of B_A be? (Show your work)

Solution: To have an amplitude resolution of $< 4\text{mV}$, we need two successive samples from a sine wave to differ by no more than 8mV . Therefore we need $\frac{2\pi}{N} \leq 4\text{mV}$, with N being the number of samples taken within one sinusoidal period. Thus we need $N \geq 785$ entries in the sine table. This means we need $B_A = \log_2 N = 10.61$ or 11 bits (rounded up).

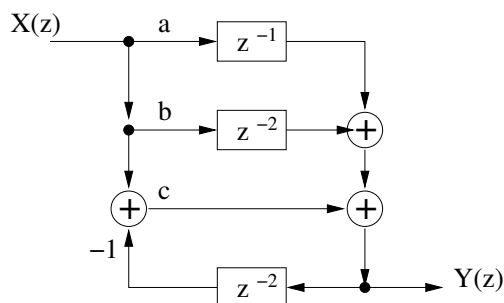
- (b) (4 pts) What should be your choice of B_D ? (Show your work)

Solution: Quantization error of 2mV means we need quantizer step size no bigger than 4mV . Thus $\frac{2}{4\text{m}} = 500$ levels in the DAC, which means we need $B_D = \log_2 500 = 8.96$ or 9 bits (rounded up).

- (c) (4 pts) What should be your choice of FTV and B_{FTV} to complete the design? (Show your work)

Solution: Here you only need to satisfy $FTV \cdot \frac{f_s}{2^{B_{FTV}}} = 300$, and $B_{FTV} > B_A = 10$. There are multiple choices. Supposing you choose $B_{FTV} = 16$, then you get $FTV = 1.966$ or 2 after rounding.

13. (18 pts) Consider the filter shown below, and assume that $a, b, c > 0$. Please show your work in answering the following questions.



- (a) (2 pts) Please derive the transfer function $H(z)$ for the above filter.

Solution:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{c + az^{-1} + bz^{-2}}{1 + cz^{-2}}$$

- (b) (3 pts) Please put the above diagram into the a standard direct form and its transposed version.

Solution: *The answer is not given here; basically you can use either DF I/II and TDF I/II.*

- (c) (3 pts) what are the values of $H(f)$ at $f = 0$, $f_s/4$ and $f_s/2$, respectively?

Solution:

i. at $f = 0$ we have $z^0 = 1$ giving

$$H(0) = (c + a + b)/(1 + c).$$

ii. at $f = f_s/4$ we have $z^{-2} = e^{-j2\pi/4} = -1$, $z^{-1} = -j$ giving

$$H(f_s/4) = \frac{c - aj - b}{1 - c}.$$

iii. at $f = f_s/2$ we have $z^{-2} = e^{-j2\pi/2} = 1$, $z^{-1} = -1$ giving

$$H(f_s/2) = \frac{c - a + b}{1 + c}.$$

- (d) (1 pt) Is this an FIR filter or IIR filter?

Solution: *IIR, due to the feedback*

- (e) (2 pt) Is this filter generally stable? If not can you give conditions on a, b, c that will ensure stability?

Solution: *Not generally stable. Need the pair of poles to be within unit circle: $|c| < 1$*

- (f) (2 pt) Under what condition of a, b, c does the filter have unity gain for a DC input? If this condition is not satisfied, how would you scale/normalize the filter so it does?

Solution: The DC input gain is $\frac{c+a+b}{1+c}$, so for it to be unity we need $a + b = 1$. If this is not the case, then we need to normalize all a, b, c by a multiplication factor of $\alpha = \frac{1}{a+b}$.

- (g) (1 pt) Where in the filter might you worry about overflow?

Solution: Three places: output of the adders.

- (h) (4 pts) Consider the following specific values: $a = 1.6, b = c = 0.8$. Please plot the pole-zero location of this filter on the z -plane, and sketch its magnitude response. Classify the filter as lowpass, highpass, bandpass, bandstop, or none of the above.

Solution: The resulting filter transfer function is easy to factorize:

$$H(z) = 0.8 \frac{z^2 + 2z + 1}{z^2 + 0.8} = 0.8 \frac{(z + 1)^2}{(z - j\sqrt{0.8})(z + j\sqrt{0.8})}$$

So we have a pair of poles at $\pm j\sqrt{0.8}$ and a pair of zeros both at -1 . This should be a lowpass filter with first zero at $F_s/2$ and peak at $F_s/2$.