Midterm — November 13, 2000

Write and sign the honor pledge.

1. (2 pts) Print your name on each sheet.
2. (10 pts) Write the equations that define the discrete Fourier transform (DFT) and the inverse discrete Fourier transform (IDFT).

3. (5) How many butterfly operations are needed when performing a radix-2 decimation-in-time FFT having 2^M input values?

4. (20 pts) The output of a quantizer is often modeled by adding an error waveform to the input to produce the quantized result. This is done on the assumption that the quantization error is independent of the input waveform. In many cases this is nearly true, in many cases it is the best, simplest model that gives a semblance of a reasonable result.

   The block diagram in Figure 1 uses such a model.

   Looking at the basic system geometry it is clear that the up-converted input signal $y_u[n]$ experiences a different transfer function than does the quantization noise $q[n]$. This difference is what makes the Delta-Sigma approach to digital-to-analog conversion useful.

   Determine the transfer functions

$$H_y(z) = \frac{Y_q(z)}{Y_u(z)}$$
$$H_q(z) = \frac{Y_q(z)}{Q(z)}.$$

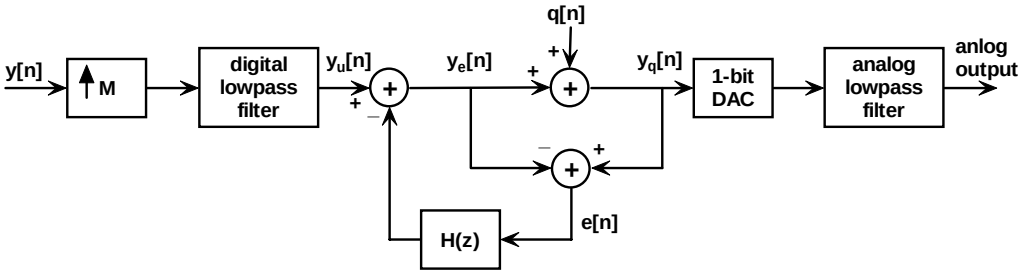

Figure 1: Delta-Sigma D/A converter.

5. (10 pts) Draw and label the block diagram that we used in class and is found in the text for the delta-sigma A/D converter.

6. (10 pts) In the DSP56303 the a accumulator is composed of more than one register.

   (a) Name the registers.

   (b) How many bits does each register contain?

   (c) Which register contains the least significant bits?

   (d) Which register contains the overflow bits?

   (e) Which register is normally used to contain fractions?

7. (10 pfs) In the TMS320C5402 the a accumulator is composed of more than one register.

   (a) Name the registers.

   (b) How many bits does each register consist of?

   (c) Which register contains the least significant bits?

   (d) Which register contains the overflow bits?

   (e) Which register is normally used to contains a fraction?

8. (20 pts) For the filter shown in Figure 2 write the equations for the transfer functions $W_2(z)/X(z)$ and $Y(z)/X(z)$.

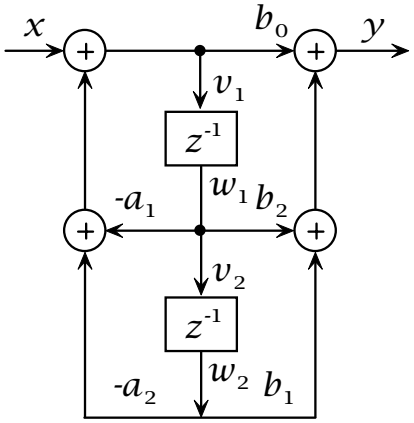

Figure 2: Direct form 2 second order section.

9. (20 pts) We used the following vector equation to develop a procudure to numerically determine the input to delay stage output transfer functions.

$$\mathbf{w}[n+1] = \mathbf{A}\mathbf{w}[n] + \mathbf{B}\mathbf{x}[n].$$

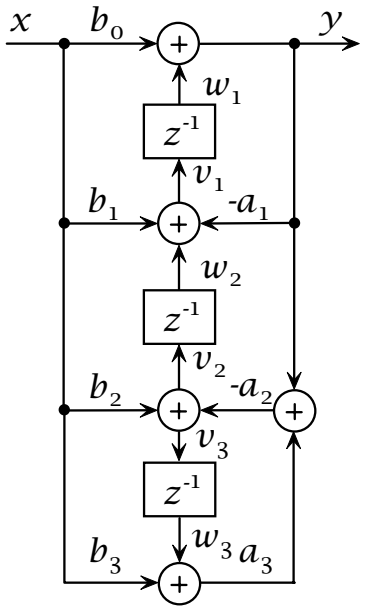

Figure 3: Unusual third order filter design.

For the filter shown in Figure 3 this can be written as

$$\begin{vmatrix} w_1[n+1] \\ w_2[n+1] \\ w_3[n+1] \end{vmatrix} = \mathbf{A} \begin{vmatrix} w_1[n] \\ w_2[n] \\ w_3[n] \end{vmatrix} + \mathbf{B} \begin{vmatrix} x \\ 0 \\ 0 \end{vmatrix}$$

Write out what the **A** and **B** matrices are for the filter shown in Figure 3.

10. (5 pts) Express z^{-1} in complex exponential form. Define your variables and their ranges of value.

11. (2 pts each) True or False

    ____ In a typical DSP processor the execution time for addition is negligible compared to the time for multiplication.

    ____ Delta-sigma D/A converters shift high frequency quantization noise to very low frequencies where it is easily filtered out using a highpass filter

    ____ Both the TMS320C5402 and the DSP56303 are "pure" Harvard architectures.

    ____ When implementing an IIR digital filter using second order sections it is best to place the sections having poles nearest the unit circle closest to the input in order to minimize the possibility of overflow effects.

    ____ FIR filters are more complicated to design than are IIR filters and thus are more difficult to design and implement.

    ____ The DSP56303 supports pre-increment indirect addressing.

    ____ The TMS320C5402 supports pre-increment indirect addressing.

    ____ Least square polynomial fits to functions result in tighter error bounds than do fits made using made using the Remez exchange algorithm.

    ____ The stack on the TMS320C5402 grows in the direction of increasing memory addresses.

    ____ The TMS320C5402 does not support a circular addressing mode.

    ____ The DSP56303 supports configuring the use of its memory under program control.

    ____ Both the TMS320C5402 and the DSP56303 use codecs that have 16-bit A/D and D/A converters.

    ____ The concept of windowing a set of sample values is to reduce leakage caused by not synchronizing the data with sample rate.

    ____ One of the Prime Factor FFT Algorithm features that makes it useful is that it converts a single dimensional DFT into a multiple dimensional DFT.

    ____ FIR filters typically possess less delay than do IIR filters having basically same filter characteristics.

___ The bit reverse addressing mode is useful when cascading biquad IIR filter stages.

___ The delta-sigma A/D converter uses an up rate converter at its output to get its processing speed.

___ When the number of values in a DFT can be factored a fast algorithm can be found to speed up calculation of the DFT values.

___ When the number of values in a DFT is prime it is not possible speed up the calculation of the DFT values.

___ IIR filter designs need to consider the likelihood of overflow however FIR filters are immune to this if their coefficient values are limited to be less than one-half in magnitude.

___ Block floating point FFT calculations are generally more accurate than floating point calculations. This is because there are more bits available in word for use as mantissa values than with a floating point format having the same word size.

___ Mathematical subroutines provided by DSP manufacturers has been carefully written and documented and can be safely used without concern.

___ The DSP56303 architecture is optimized for the decimation-in-frequency FFT algorithm.

___ Patents can only be renewed once. After that they are in the public domain.

12. (20 pts)

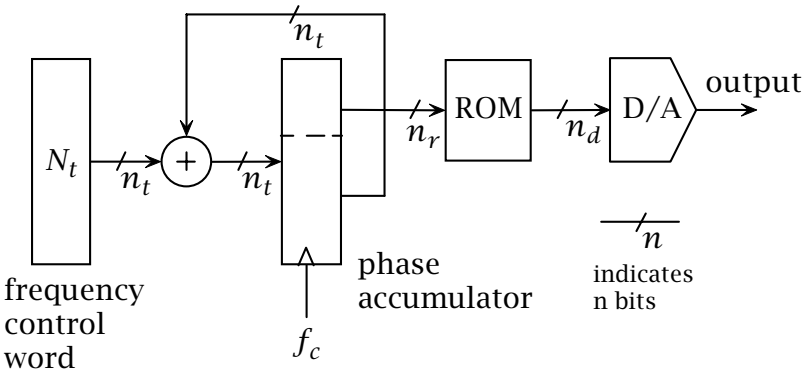

Figure 4: Direct digital waveform synthesizer.

A direct digital waveform generator is shown in Figure 4. Assume that the ROM contains samples of one period of a sine wave. The ROM is addressed

using the n_r most significant bits in the n_t bit accumulator The number of bits used to synthesize the sinewave waveform is n_d. The frequency control (or tuning) word value is N_t.

(a) (5) What is the smallest step size between possible output frequencies?

(b) (5) What value of input turning value, N_t, will generate the maximum output frequency?

(c) (10) What is the maximum signal-to-noise ratio at the D/A output for the sinewave due to amplitude quantization?

13. (5 pts) How many zero values are needed to be inserted between samples of a sampled data stream in order to increase the sample rate by a factor of 7?

14. (5 pts) List the names of the auxiliary registers on the TMS320C5402. What is the primary function of these registers?

15. (15 pts) List the names of the registers used on the DSP56303 for indexing and indexing arithmetic. Indicate the primary function of each class of registers.

16. (5 pts) How many words of on-chip memory are present on the TMS320C5402?

17. (5 pts) How many words of on-chip memory are present on the DSP56303?

18. (5 pts) On the DSP56303 which of the address registers was reserved by us for use as the stack pointer?

19. (5 pts) On the TMS320C5402 what is the name of the register used as the stack pointer?

20. (5 pts) Write a line of code to accomplish the following on the C5402: execute a function call assuming that the low word of `b` accumulator contains the address of the function to be called.

21. (5 pts) On the C5402, what is the primary difference between the `mac` and `mas` instructions?

22. (10 pts) The MATLAB SPTOOL offers four named IIR implementations. Of these we looked at three and carried only one through to completion What is the name of the filter that

    (a) has ripple in both the passband and the stopband:

    (b) has ripple in the passband but no ripple in the stopband:

(c) has a monotone roll off in the passband and ripple in the stopband:

(d) SPTOOL advised us would require too many poles to be easily relized:

(e) required the lesser number of stages:

23. (10 pts) If we multiply a Q1.23 format fractional number by a Q2.22 on the Motorola DSP56303

(a) the result in the full accumulator is a Qn.m number. What are the values of n and m?

(b) the result is moved from the middle word of the accumulator. What are the n and m values in the moved value?

24. (10 pts) Show how fractional values (word size, sign and binary point) are organized in a word for

(a) TMS320C542 using Q1.15 format:

(b) DSP56303 using Q8.16 format:

25. (5 pts) In the TMS320C5402 what is the function of the OVM bit?

26. (5 pts) In lab and class we (the instructor) were tardy in determining maximum input voltage range to the TMS320C5402 was without clipping. This was important is setting the levels when testing our IIR implementations. The reported limiting input voltage in volts peak-to-peak was

27. (20 pts) We looked at the advantages of representing DFT index values using various mappings.

    (a) One mapping that we looked at used the form

    $$k = k_1 + k_2 N_1 \quad \text{and} \quad n = n_1 N_2 + n_2$$

    where the number of values in the DFT was $N = N_1 N_2$. How many complex multiply operations result using only this mapping.

    (b) I gave an example of the reduction of the number of complex multiply operations that resulted using the prime factor algorithm as compared to the DFT definition. The value of N that I used was $8184 = 3 \times 8 \times 11 \times 31$. What was the factor by which the number of complex multiply operations was reduced?

28. (18 pts) The following instruction

    ```
    ld  *pd+%,16,a
    ```

    uses `pd` as alias for AR2. The contents of `AR2` is 0454h.

    (a) What memory location or accumulator register is the source of the value to be loaded?

    (b) What memory location or accumulator register is the destination of this instruction?

    (c) What does the * denote?

(d) What does the + denote?

(e) What does the 16 denote?

(f) What does the % denote?

29. (15 pts) There are generally four primary uses of the stack by a function or subroutine such as IIRCAS5. Three of these are:

(a)

(b)

(c)

30. (5 pts) The *overlap-and-save* method is a means of computing the outputs of a P-stage FIR filter using a N value FFT on block fashion. How many values filter output values are generated per block (assume $N > P$)?