Midterm — November 14, 2001

Write and sign the honor pledge.

1. (2 pts) Print your name on *each* sheet.
2. (10 pts) Write the equations that define the discrete Fourier transform (DFT) and the inverse discrete Fourier transform (IDFT). Do not use the letter W in your answer.

   Forward transform:

   Inverse transform:

3. (10 pts) As part of the prelab for the second week of the C5402 lab exercise we used FDATool to generate a list of coefficient values for use in programming a FIR filter in C. The values generated by the FDATool program all had magnitudes less than one. In order to use these values in C we converted the values into Q15 (also known as Q0.15) values and represented them as signed 16 bit integers. This was simply done by multiplying them by a constant and then discarding the fractional parts.

   What was that constant?

4. (20 pts) The state matrix equations for the second order filter section shown in Figure 1 can be writen in matrix form as

$$\begin{aligned} \mathbf{w}[n+1] &= \mathbf{A}\mathbf{w}[n] + \mathbf{B}\mathbf{x}[n] \\ \mathbf{y}[n] &= \mathbf{C}\mathbf{w}[n] + \mathbf{D}\mathbf{x}[n]. \end{aligned}$$

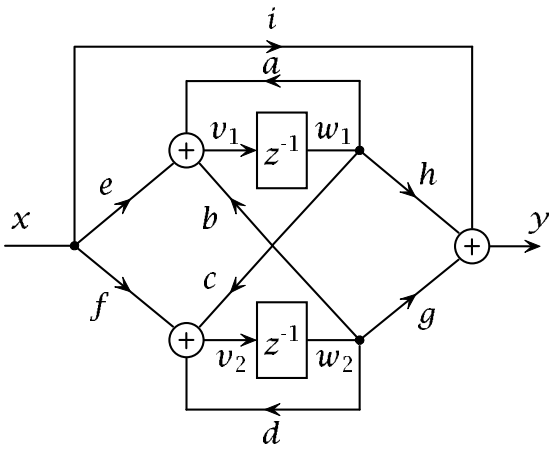

Figure 1: Second order filter section.

Write the **A**, **B**, **C**, and **D** matrices in terms of a, b, c, d, e, f, g, h, and i.

5. Figure 2 contains a plot of a magnitude and phase measurement using the Tektronix 2642A Personal Spectrum Analyzer located in the lab.

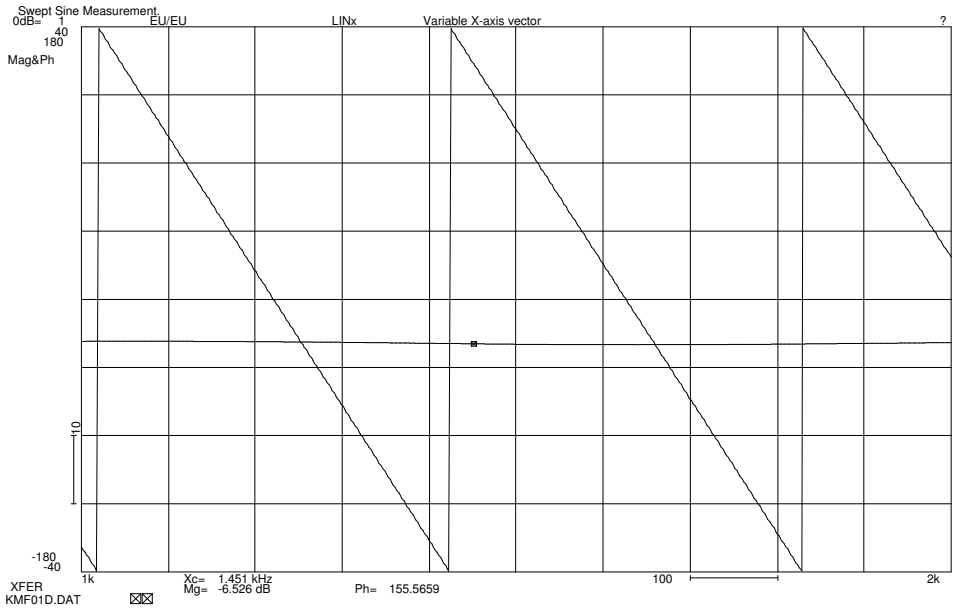

Figure 2: Phase measurement made using the Tektronix 2642A.

What is the estimated group delay in seconds?

6. (30pts) Figure 3 shows a biquad section that we want to implement on the TMS320C5402.

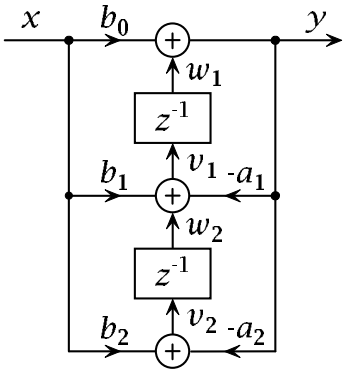

Figure 3: Biquad filter section.

Several of the auxiliary registers are renamed using the following aliases:

`ptr_x`	points to the input values
`ptr_w`	points to the delay stage contents
`ptr_h`	points to the coefficient array
`ptr_y`	points to the output array
`ptr_t`	points to a temporary register

The coefficient array holds both the a and b values. It may be organized as needed to facilitate program flow. The a_1 and b_1 values stored in the coefficient array will have been divided by two. This needs to be corrected for in the code.

Write the code that would form the inner loop of a function that implements a IIR filter as the cascade as a number of these biquad sections. This involves computing a y value, updating the delay stage contents and setting up for the next loop. The temporary register is used as the input to each section and also needs to be updated. Include comments indicating when using coefficient values which values are being used.

7. (30 pts) For the filter shown in Figure 4 write the equations for the transfer functions $Y(z)/X(z)$, $W_1(z)/X(z)$, and $W_2(z)/X(z)$ in terms of the coefficient values. No need to place terms over a common denominator.

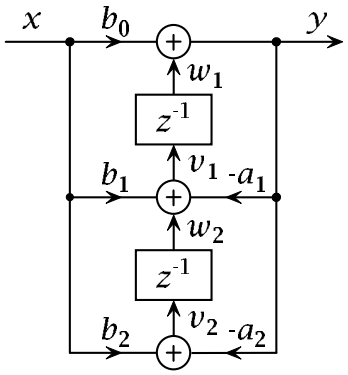

Figure 4: Biquad section block diagram.

8. (10 pts) The direct digital frequency synthesizer (Figure 5) is finding increasing use in test and communication hardware.

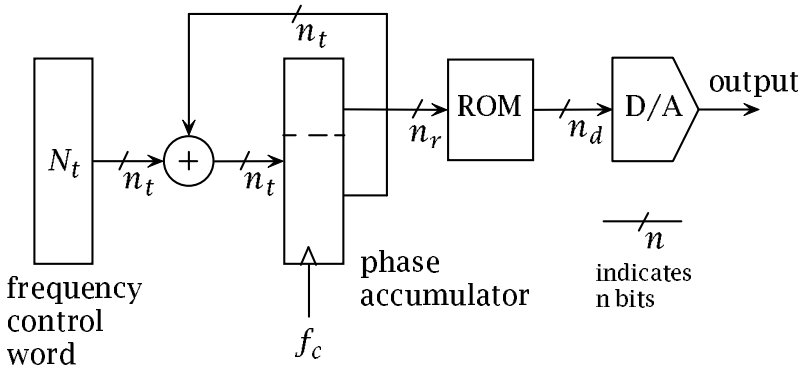

Figure 5: Direct digital frequency synthesizer block diagram.

Both the register holding the frequency tuning word (FTW) and the accumulator are n_t bits in length. The read only memory (ROM) is assumed to hold samples of one complete period of a sinewave.

Assume that the accumulator is clocked at a rate of 1MHz. $n_t = 10$ bits.

What is the frequency that results using a FTW value of 89 (decimal)?

9. Assume a set of samples obtained using a sample rate of f_s, over T seconds, consisting of N samples.

   (a) (5 pts) What is the frequency step size in Hz between values in the DFT of the given data set?

   (b) (5 pts) The size of the data set is expanded by adding five zeros following each original sample. What is the frequency step size in Hz between values in the DFT of the resulting set of values?

   (c) (5 pts) The size of the data set is expanded by appending a total of $5N$ zeros to the end of the data set. What is the frequency step size in Hz between values in the DFT of the augmented set of values?

10. (20 pts) The C5402 possess 16 “indirect” addressing modes. These have the following syntactic forms:

a) `*ARx`
b) `*ARx-`
c) `*ARx+`
d) `*+ARx`
e) `*ARx-0B`
f) `*ARx-0`
g) `*ARx+0`
h) `*ARx+0B`
i) `*ARx-%`
j) `*ARx-0%`
k) `*ARx+%`
l) `*ARx+0%`
m) `*ARx(lk)`
n) `*+ARx(lk)`
o) `*+ARx(lk)%`
p) `*(lk)`

Match the above syntax descriptions to the following descriptions (where IA=indirect address, BR=bit reverse):

____ IA post subtract c(AR0) circular
____ pre-increment IA
____ pre-increment IA pointing to C(ARn) + lk
____ IA post decrement circular
____ use absolute memory address lk
____ IA post add c(AR0)
____ IA pointing to C(ARn) + lk
____ IA post subtract c(AR0)
____ IA post decrement by 1
____ IA post BR add c(AR0)

11. (20 pts) There are four primary uses of the stack by a function or subroutine such as IIRCAS5. These are:

    (a)

    (b)

    (c)

    (d)

12. (10 pts) In the DSP56303 the A accumulator is composed of more than one register.

    (a) Name the registers.

    (b) How many bits does each register contain?

    (c) Which register contains the least significant bits?

    (d) Which register contains the overflow bits?

    (e) Which register is normally used to contain fractions?

13. (10 pfs) In the TMS320C5402 the A accumulator is composed of more than one register.

    (a) Name the registers.

(b) How many bits does each register consist of?

(c) Which register contains the least significant bits?

(d) Which register contains the overflow bits?

(e) Which register is normally used to contains a fraction?

14. (5 pts) Express z^{-1} in complex exponential form. Define your symbols and their units and/or ranges of value.

15. (2 pts each) True or False

____ In a typical DSP processor the execution time for addition is negligible compared to the time for multiplication.

____ Both the TMS320C5402 and the DSP56303 are "pure" Harvard architectures.

____ When implementing an IIR digital filter using second order sections it is best to place the sections having poles nearest the unit circle closest to the input in order to minimize the possibility of overflow effects.

____ FIR filters are more complicated to design than are IIR filters and thus are more difficult to design and implement.

____ The DSP56303 supports pre-increment indirect addressing.

____ The TMS320C5402 supports pre-increment indirect addressing.

____ Least square polynomial fits to functions result in tighter error bounds than do fits made using made using the Remez exchange algorithm.

____ The stack on the TMS320C5402 grows in the direction of decreasing memory addresses.

____ The TMS320C5402 does not support a circular addressing mode.

____ The DSP56303 supports configuring the use of its memory under program control.

____ Both the TMS320C5402 DSK and the DSP56303EVM contain CODECs that have 16-bit A/D and D/A converters.

____ The concept of windowing a set of sample values is used to reduce leakage caused by not synchronizing the data with sample rate.

____ The bit reverse addressing mode is useful when cascading biquad IIR filter stages.

____ IIR filter designs need to consider the likelihood of overflow however FIR filters are immune to this if their coefficient values are limited to be less than one-half in magnitude.

____ Mathematical subroutines provided by DSP manufacturers have been carefully written and documented and can be safely used without concern.

____ The MATLAB `fftshift` function is very useful because it combines calculating the FFT of a data set with rotation of the result to place zero frequency at the midpoint of the array holding the result.

16. (5 pts) List the names of the auxiliary registers on the TMS320C5402. What is the primary function of these registers?

17. (15 pts) List the names of the registers used on the DSP56303 for indexing and indexing arithmetic. Indicate the primary function of each class of registers.

18. (5 pts) How many words of on-chip memory used to hold program/data are present on the TMS320C5402?

19. (5 pts) Into how many blocks is the TMS320C5402 memory divided into and how many simultaneous memory accesses can there be to each block?

20. (5 pts) How many words of on-chip memory are present on the DSP56303?

21. How many on-chip memory words are contained in each address space on the DSP56303 (default configuration).

22. (5 pts) On the DSP56303 which of the address registers was reserved by us for use as the stack pointer?

23. (5 pts) On the TMS320C5402 what is the name of the register used as the stack pointer?

24. (10 pts) The MATLAB FDATool offers four named IIR implementations. Of these we looked at three and carried only one through to completion What is the name of the filter that

    (a) has ripple in both the passband and the stopband:

    (b) has ripple in the passband but no ripple in the stopband:

    (c) has a monotone roll off in the passband and ripple in the stopband:

    (d) the filter type that we did not use because of the large number of delays needed to implement it:

(e) required the lesser number of stages:

25. (10 pts) If we multiply a Q0.23 format fractional number by a Q3.20 on the Motorola DSP56303

(a) the result in the full accumulator is a Qn.m number. What are the values of n and m?

(b) the result is moved from the middle word of the accumulator. What are the n and m values for the moved value?

26. (10 pts) For a hypothetical DSP having a 10 bit word size write in binary the bit patterns that correspond to the

(a) positive integer value 12.5 using Q4.5 format

(b) negative integer value 12.5 using Q4.5 format

(c) positive fractional value 0.75 using Q6.3 format

(d) negative fractional value 0.75 using Q6.3 format

(e) positive fractional value 0.125 using Q0.9 format

27. (20 pts) In the TMS320C5402 what is the function of the following status bits

(a) `OVM`

(b) SXM

(c) FRCT

(d) SST

28. (15 pts)

(a) The *overlap-and-save* method is a means of computing the outputs of a *P*th order FIR filter (P+1 delay stages) using a *N* value FFTs. How many new input values are required per transform block (assume that $N > P$)?

(b) Which values are saved between transforms?

(c) Where are the saved values placed prior to forming the next transform?