Midterm/Final Exam — March 20, 2000

Write and sign the honor pledge.

1. (2 pts) Print your name on each sheet.
2. (5 pts) Several times during the semester I drew a block diagram that shows the *essence of digital signal processing*. Draw and label it.
3. (10 pts) There were five structured lab exercises. For each lab exercise list main topic of the lab exercise and one additional topic that was a focus.

   (a)

   (b)

   (c)

   (d)

   (e)
4. (10 pts) Write the equations that define the discrete Fourier transform (DFT) and the inverse discrete Fourier transform (IDFT).

5. (20 pts) The output of a quantizer is often modeled by adding an error waveform to the input to produce the quantized result. This is done on the assumption that the quantization error is independent of the input waveform. In many cases this is nearly true, in many cases it is the best, simplest model that gives a semblance of a reasonable result.

   The block diagram in Figure 1 uses such a model.

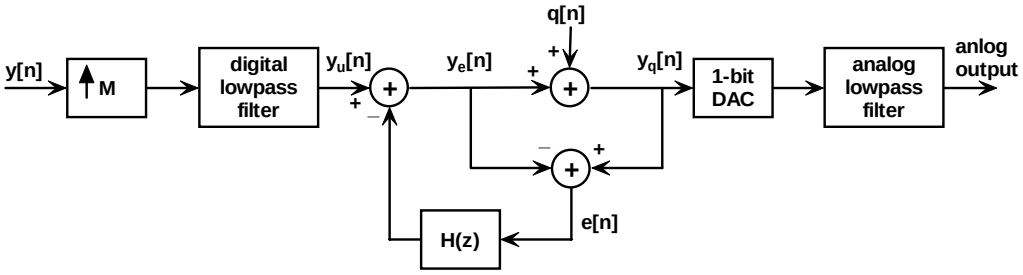

Figure 1: Delta-Sigma D/A converter.

Looking at the basic system geometry it is clear that the up-converted input signal $y_u[n]$ experiences a different transfer function than does the quantization noise $q[n]$. This difference is what makes the Delta-Sigma approach to digital-to-analog conversion useful.

Determine the transfer functions

$$H_y(z) = \frac{Y_q(z)}{Y_u(z)}$$

$$H_q(z) = \frac{Y_q(z)}{Q(z)}.$$

6. (5 pts) What is transfer saturation?

7. (5 pts) For the DSP56303 write an instruction to move a fractional value from the a register without causing a saturated transfer?

8. (10 pts) In the DSP56303 the a accumulator is composed of more than one register.

   (a) Name the registers.

   (b) How many bits does each register consist of?

   (c) Which register contains the least significant bits?

   (d) Which register contains the overflow bits?

   (e) Which register normally contains a fraction?

9. (10 pfs) In the TMS320C542 the a accumulator is composed of more than one register.

   (a) Name the registers.

   (b) How many bits does each register consist of?

   (c) Which register contains the least significant bits?

   (d) Which register contains the overflow bits?

   (e) Which register normally contains a fraction?

10. (5 pts) For the TMS320C542 what is the instruction used to saturate the b accumulator.

11. (5 pts) What does the MATLAB function `fftshift` do? Does it form a FFT as one of its processing steps?

12. (20 pts) For the filter shown in Figure 2 write the equations for the transfer functions $V1(z)/X(z)$ and $Y(z)/X(z)$.

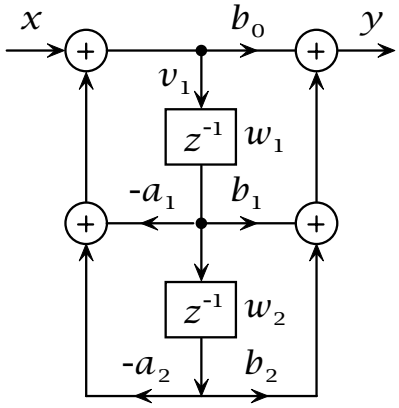

Figure 2: Direct form 2 biquad stage

13. (20 pts) Figure 3 contains the block diagram of a transposed direct form II biquad stage.

    Write the equations for transfer functions $V1/X(z)$ and $V2(z)/X(z)$ in terms of the transfer function $Y(z)/X(z)$.

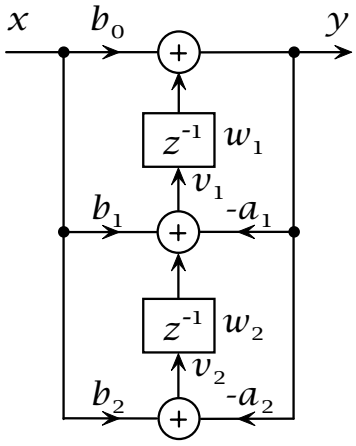

Figure 3: Transposed form 2 biquad stage

14. (2 pts each) True or False

___ In the DSP56303 the interrupt vector is fixed in memory and cannot be relocated.

___ In the TMS320C542 the interrupt vector is fixed in memory and cannot be relocated.

___ In a typical DSP processor the execution time for addition is negligible compared to the time for multiplication.

___ TMS320C542 auxiliary register `AR7` is normally used as a stack pointer.

___ DSP56303 auxiliary register `R6` is normally used as a stack pointer.

___ Delta-sigma D/A converters shift high frequency quantization noise to very low frequencies where it is easily filtered out using a highpass filter

___ The TMS320C542 uses dual access random access memory for holding data and single access random access memory for holding program.

___ Neither the TMS320C542 nor the DSP56303 are “pure” Harvard architectures. However the C542 is closer to the ideal than is the 303.

___ In implementing an IIR digital filter using biquad stages it is best to place the high-Q stages closer to the input in order to minimize their overlow effects on the output.

___ FIR filters have more aspects to their design than do IIR filters and thus are more difficult to design and implement.

___ Limit cycles can be caused by quantization of data values in FIR filter.

___ Least square polynomial fits to functions result in tighter error bounds than do fits made using made using the Remez exchange algorithm.

___ The TMS320C542 does not support a circular addressing mode.

___ The DSP56303 supports configuring the use of its memory under program control.

___ Both the TMS320C542 and the DSP56303 use codecs that have 16-bit A/D and D/A converters.

___ The concept of windowing a spectrum is to reduce leakage caused by not synchronizing the data with sample rate.

___ One of the Prime Factor FFT Algorithm features that makes it useful is that it converts a single dimensional DFT into a multiple dimensional DFT.

___ FIR filters typically possess less delay than do reasonably equivalent IIR filters.

____ The bit reverse addressing mode is useful when cascading biquad IIR filter stages.

____ The delta-sigma A/D converter uses a up rate converter to get it's processing speed.

____ There are no operational restrictions on programming the AC01C B register. However, the A register must be loaded with a value greater than 10.

____ IIR filters are more likely to cause waveform distortion than will symmetric FIR filters because of the differences in their phase characteristics.

____ IIR filter designs need to consider the likelihood of overflow however FIR filters are immune to this if their coefficient values are limited to be less than one-half in magnitude.

____ The DSP56303 architecture is optimized for the decimation-in-frequency FFT algorithm.

____ Patents can only be renewed once. After that they are in the public domain.

15. (10 pts) On the DSKplus the clock to the TLC320AC01C codec whip is 10^6 Hz. The cutoff frequency of the switched capacitor filter on the AC01C and the sample frequency are set by registers named A and B.

    (a) What is the equation defining the filter cutoff frequency to the input frequency, A contents, and B contents?

    (b) What is the equation defining the sampling frequency to the input frequency, A contents, and B contents?

16. (5 pts) What is the sample rate normally used in the lab exercises using the CS4215 codec chip on the DSP56303EVM?

17. (5 pts) List the names of the auxiliary registers on the TMS320C542. What is the primary function of these registers?

18. (5 pts) List the names of the registers used on the DSP56303 for indexing and indexing arithmetic. Indicate the primary function of each class of registers.

19. (5 pts) How many words of on-chip memory present on the TMS320C542?

20. (5 pts) How many words of on-chip memory present on the DSP56303?

21. (10 pts) Using the MATLAB SPTOOL we considered four IIR implementations. Of these we carried three filter designs through to completion for the IIR laboratory exercise. Name the filter that

    (a) has ripple in both the passband and the stopband:

    (b) has ripple in the passband but no ripple in the stopband:

    (c) has a monotone roll off in the passband and ripple in the stopband:

    (d) SPTOOL advised us against using:

    (e) required the lesser number of stages:

22. (4) In lab and class we demonstrated problems associated with the instruction pipeline.

    (a) Which processor demonstrated a problem with accessing values in the pipeline before they were ready?

    (b) Which processor demonstrated a problem with restarting a flushed pipeline after an interrupts?

23. (10 pts) Show how fractional values (word size, sign and binary point) are organized in a word for

    (a) TMS320C542:

    (b) DSP56303:

24. (10 pts) Draw the basic butterfly for the decimation-in-time FFT and for the decimation-in-time FFT indicating where the *twiddle factors* go.

25. (5 pts) In EECS 452 we cover two somewhat dissimilar DSP processors. It has been suggested we focus on one processor instead. The issue is broad coverage vs depth. In your opinion would the course be improved by focusing on a single processor?