Midterm — March 26, 2001

Write and sign the honor pledge.

1. (2 pts) Print your name on each sheet.
2. (10 pts) Write the equations that define the discrete Fourier transform (DFT) and the inverse discrete Fourier transform (IDFT).

3. (10 pts) Draw and label the block diagram that we used in class, used for Homework 4, and is found in the text for the delta-sigma D/A converter.

4. (30 pts) For the second order delta-sigma A/D shown in Figure 2 determine the transfer functions

$$\frac{Y(z)}{X(z)}$$
$$\frac{Y(z)}{E(z)}.$$

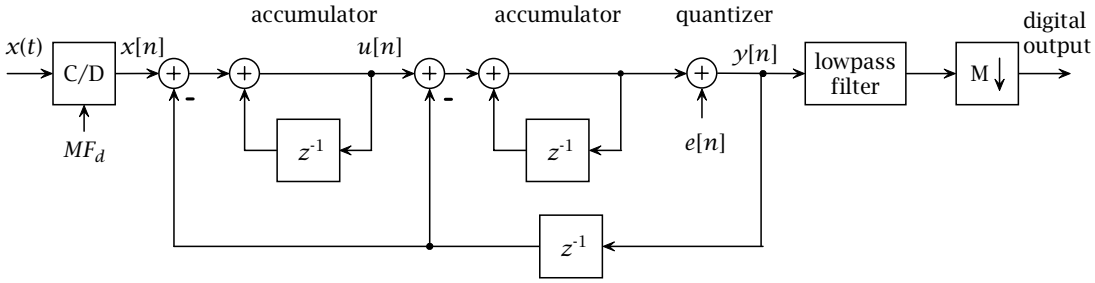

Figure 1: Second order delta-sigma A/D converter model.

Hint: determine the individual accumulator transfer functions first.

5. Assume a set of samples obtained using a sample rate of f_S, over T seconds, consisting of N samples.

   (a) (5 pts) What is the frequency step size in Hz between values in the DFT of the given data set?

   (b) (5 pts) The size of the data set is expanded by placing three zeros between each original sample. What is the frequency step size in Hz between values in the DFT of the resulting set of values?

   (c) (5 pt) The size of the data set is expanded by appending a total of $3N$ zeros to the end of the data set. What is the frequency step size in Hz between in the DFT of the resulting set of values?

6. (20 pts) Figure 3 contains the block diagram of a third order *Normal* IIR filter.

   This filter structure is reputed to have low sensitivity to the quantization of its coefficient (the a, b, c, d, and e) values. The price for this is complexity.

   We wish to compute the transfer functions from the input x to the outputs (y_1, y_2, and y_3) of the three delay stages.

   Recall that for a delay stage we have $y_k[n+1] = w_k[n]$.

   The updating of the state of this filter can be written in matrix form as

$$\mathbf{y}[n+1] = \mathbf{A}\mathbf{y}[n] + \mathbf{B}\mathbf{x}[n].$$

   Taking the z-transform and solving we have (assuming a single x input)

$$\frac{\mathbf{Y}(z)}{X(z)} = (z\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}$$

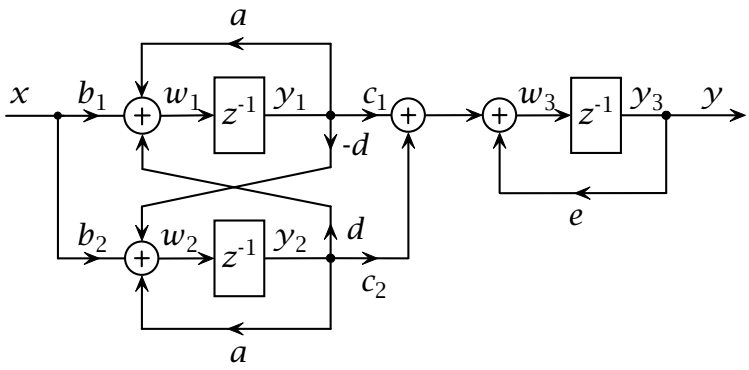

Figure 2: Third order Normal filter.

In less compact form we have

$$\begin{bmatrix} y_1[n+1] \\ y_2[n+1] \\ y_3[n+1] \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \begin{bmatrix} y_1[n] \\ y_2[n] \\ y_3[n] \end{bmatrix} + \begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} x$$

For the Normal filter shown in Figure 3 write down the **A** and **B** matrices.

7. (20 pts) The C5402 possess 16 "indirect" addressing modes. These have the following syntactic forms:

a) `*ARx`
b) `*ARx-`
c) `*ARx+`
d) `*+ARx`
e) `*ARx-0B`
f) `*ARx-0`
g) `*ARx+0`
h) `*ARx+0B`
i) `*ARx-%`
j) `*ARx-0%`
k) `*ARx+%`
l) `*ARx+0%`
m) `*ARx(lk)`
n) `*+ARx(lk)`
o) `*+ARx(lk)%`
p) `*(lk)`

Match the above syntax descriptions to the following descriptions (where IA=indirect address, BR=bit reverse):

____ IA post subtract c(AR0) circular
____ pre-increment IA
____ pre-increment IA pointing to C(ARn) + lk
____ IA post decrement circular
____ use absolute memory address lk
____ IA post add c(AR0)
____ IA pointing to C(ARn) + lk
____ IA post subtract c(AR0)
____ IA post decrement by 1
____ IA post BR add c(AR0)

8. (10 pts) In the DSP56303 the A accumulator is composed of more than one register.

(a) Name the registers.

(b) How many bits does each register contain?

(c) Which register contains the least significant bits?

(d) Which register contains the overflow bits?

(e) Which register is normally used to contain fractions?

9. (10 pfs) In the TMS320C5402 the A accumulator is composed of more than one register.

   (a) Name the registers.

   (b) How many bits does each register consist of?

   (c) Which register contains the least significant bits?

   (d) Which register contains the overflow bits?

   (e) Which register is normally used to contains a fraction?

10. (20 pts) For the filter shown in Figure 4 write the equations for the transfer functions $V_1(z)/X(z)$ and $Y(z)/X(z)$.

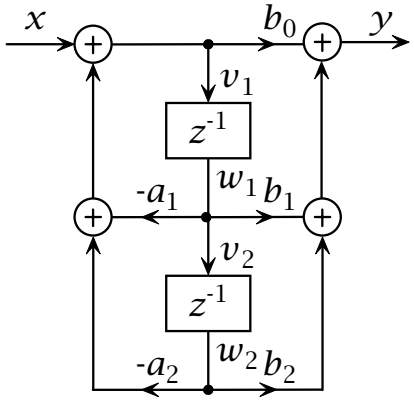

Figure 3: Filter block diagram.

11. (5 pts) Express z^{-1} in complex exponential form. Define your symbols and their values and/or ranges of value.

12. (2 pts each) True or False

    ____ In a typical DSP processor the execution time for addition is negligible compared to the time for multiplication.

    ____ Delta-sigma D/A converters shift high frequency quantization noise to very low frequencies where it is easily filtered out using a highpass filter

    ____ Both the TMS320C5402 and the DSP56303 are "pure" Harvard architectures.

    ____ When implementing an IIR digital filter using second order sections it is best to place the sections having poles nearest the unit circle closest to the input in order to minimize the possibility of overflow effects.

    ____ FIR filters are more complicated to design than are IIR filters and thus are more difficult to design and implement.

____ The DSP56303 supports pre-increment indirect addressing.

____ The TMS320C5402 supports pre-increment indirect addressing.

____ Least square polynomial fits to functions result in tighter error bounds than do fits made using made using the Remez exchange algorithm.

____ The stack on the TMS320C5402 grows in the direction of increasing memory addresses.

____ The TMS320C5402 does not support a circular addressing mode.

____ The DSP56303 supports configuring the use of its memory under program control.

____ Both the TMS320C5402 and the DSP56303 use CODECs that have 16-bit A/D and D/A converters.

____ The concept of windowing a set of sample values is used to reduce leakage caused by not synchronizing the data with sample rate.

____ FIR filters typically possess less delay than do IIR filters having basically same filter characteristics.

____ The bit reverse addressing mode is useful when cascading biquad IIR filter stages.

____ The delta-sigma A/D converter uses an up rate converter at its output to get its processing speed.

____ When the number of values in a DFT can be factored a fast algorithm can be found to speed up calculation of the DFT values.

____ When the number of values in a DFT is prime it is not possible speed up the calculation of the DFT values.

____ IIR filter designs need to consider the likelihood of overflow however FIR filters are immune to this if their coefficient values are limited to be less than one-half in magnitude.

____ Mathematical subroutines provided by DSP manufacturers has been carefully written and documented and can be safely used without concern.

13. (20 pts)

A direct digital waveform generator is shown in Figure 5. Assume that the ROM contains samples of one period of a sine wave. The ROM is addressed using the n_r most significant bits in the n_t bit accumulator The number of bits used to synthesize the sinewave waveform is n_d. The frequency control (or tuning) word value, N_t, uses n_t bits.

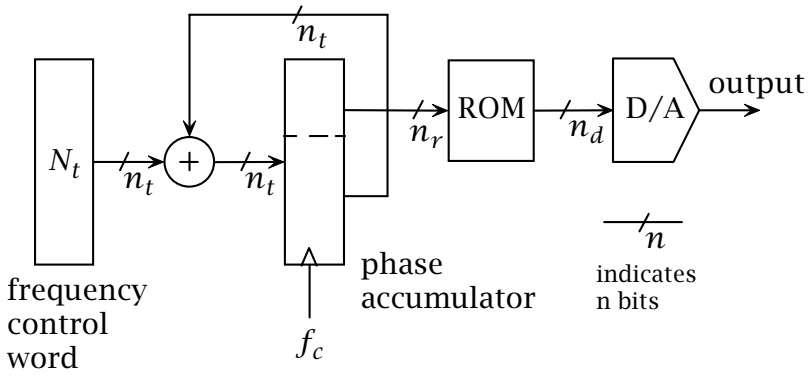

Figure 4: Direct digital waveform synthesizer.

(a) (5 pts) What is the smallest step size between possible output frequencies?

(b) (5 pts) What value of input tuning value, N_t, will generate the maximum frequency sinewave?

(c) (10 pts) What is the maximum signal-to-noise ratio at the D/A output for the output sinewave due to amplitude quantization? Assume that the D/A quanta step size is Δ. A ratio will suffice, no need to express the result in dB.

14. (5 pts) How many zero values are needed to be inserted between samples of a sampled data stream in order to increase the sample rate by a factor of 7?

15. (5 pts) List the names of the auxiliary registers on the TMS320C5402. What is the primary function of these registers?

16. (15 pts) List the names of the registers used on the DSP56303 for indexing and indexing arithmetic. Indicate the primary function of each class of registers.

17. (5 pts) How many words of on-chip memory used to hold program/data are present on the TMS320C5402?

18. (5 pts) How many words of on-chip memory are present on the DSP56303?

19. (5 pts) On the DSP56303 which of the address registers was reserved by us for use as the stack pointer?

20. (5 pts) On the TMS320C5402 what is the name of the register used as the stack pointer?

21. (5 pts) On the C5402, what is the primary difference between the `mac` and `mas` instructions?

22. (10 pts) The MATLAB SPTOOL offers four named IIR implementations. Of these we looked at three and carried only one through to completion What is the name of the filter that

(a) has ripple in both the passband and the stopband:

(b) has ripple in the passband but no ripple in the stopband:

(c) has a monotone roll off in the passband and ripple in the stopband:

(d) the filter type that we did not use because of the large number of delays needed to implement it:

(e) required the lesser number of stages:

23. (10 pts) If we multiply a Q24.23 format fractional number by a Q24.22 on the Motorola DSP56303

(a) the result in the full accumulator is a Qn.m number. What are the values of n and m?

(b) the result is moved from the middle word of the accumulator. What are the n and m values in the moved value?

24. (8 pts) In the C5402 write in hex or binary the bit patterns that correspond to the

(a) positive integer value 12

(b) negative integer value 12

(c) positive fractional value 0.75

(d) negative fractional value 0.75

25. (20 pts) In the TMS320C5402 what is the function of the following status bits

(a) OVM

(b) SXM

(c) FRCT

(d) SST

26. (18 pts) The following C5402 instruction

```
ld  *pd+%,16,a
```

uses pd as alias for AR2. The contents of AR2 is 0454h.

(a) What memory location or accumulator register is the source of the value to be loaded?

(b) What memory location or accumulator register is the destination of this instruction?

(c) What does the * denote?

(d) What does the + denote?

(e) What does the 16 denote?

(f) What does the % denote?

27. (15 pts) There are three primary uses of the stack by a function or subroutine such as IIRCAS5. These are:

(a)

(b)

(c)

28. (5 pts) The *overlap-and-save* method is a means of computing the outputs of a P-stage FIR filter using a N value FFT on block fashion. How many values filter output values are generated per block (assume that $N > P$)?