

TMS320C5515/14/05/04 DSP Real-Time Clock (RTC)

User's Guide



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Read This First

About This Manual

This document describes real-time clock (RTC) on the TMS320C5515/14/05/04 Digital Signal Processor (DSP).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
 - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
 - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320C5515/14/05/04 Digital Signal Processor (DSP) Digital Signal Processor (DSP). Copies of these documents are available on the internet at <http://www.ti.com>.

SWPU073 — TMS320C55x 3.0 CPU Reference Guide. This manual describes the architecture, registers, and operation of the fixed-point TMS320C55x digital signal processor (DSP) CPU.

SPRU652 — TMS320C55x DSP CPU Programmer's Reference Supplement. This document describes functional exceptions to the CPU behavior.

SPRUFO1A — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Inter-Integrated Circuit (I2C) Peripheral User's Guide. This document describes the inter-integrated circuit (I2C) peripheral in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The I2C peripheral provides an interface between the device and other devices compliant with Phillips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. This document assumes the reader is familiar with the I2C-bus specification.

SPRUFO2 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Timer/Watchdog Timer User's Guide. This document provides an overview of the three 32-bit timers in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The 32-bit timers of the device are software programmable timers that can be configured as general-purpose (GP) timers. Timer 2 can be configured as a GP, a Watchdog (WD), or both simultaneously.

SPRUFO3 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Serial Peripheral Interface (SPI) User's Guide. This document describes the serial peripheral interface (SPI) in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to four SPI slave devices. The SPI can operate as a master device only.

- [SPRUFO4](#) — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) General-Purpose Input/Output (GPIO) User's Guide.** This document describes the general-purpose input/output (GPIO) on the TMS320C5515/14/05/04/VC05/VC04 digital signal processor (DSP) devices. The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of an internal register. When configured as an output you can write to an internal register to control the state driven on the output pin.
- [SPRUFO5](#) — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Universal Asynchronous Receiver/Transmitter (UART) User's Guide.** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU.
- [SPRUFPI](#) — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Successive Approximation (SAR) Analog to Digital Converter (ADC) User's Guide.** This document provides an overview of the Successive Approximation (SAR) Analog to Digital Converter (ADC) on the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The SAR is a 10-bit ADC using a switched capacitor architecture which converts an analog input signal to a digital value.
- [SPRUFPI3](#) — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Liquid Crystal Display Controller (LDC) User's Guide.** This document describes the liquid crystal display controller (LDC) in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The LCD controller includes a LCD Interface Display Driver (LIDD) controller.
- [SPRUGU6](#)— TMS320C5515/14/05/04 DSP External Memory Interface (EMIF) User's Guide.** This document describes the operation of the external memory interface (EMIF) in the TMS320C5515/14/05/04 Digital Signal Processor (DSP) devices. The purpose of the EMIF is to provide a means to connect to a variety of external devices.
- [SPRUFX2](#)— TMS320C5515/14/05/04 Digital Signal Processor (DSP) Real-Time Clock (RTC) User's Guide.** This document describes the operation of the Real-Time Clock (RTC) module in the TMS320C5515/14/05/04 Digital Signal Processor (DSP) devices. The RTC also has the capability to wake-up the power management and apply power to the rest of the device through an alarm, periodic interrupt, or external WAKEUP signal.
- [SPRUFX4](#)— TMS320C5515/14/05/04 Digital Signal Processor (DSP) Inter-IC Sound (I2S) Bus User's Guide.** This document describes the features and operation of Inter-IC Sound (I2S) Bus in the TMS320C5515/14/05/04 Digital Signal Processor (DSP) devices. This peripheral allows serial transfer of full duplex streaming data, usually streaming audio, between DSP and an external I2S peripheral device such as an audio codec.
- [SPRUFX5](#)— TMS320C5515 DSP System User's Guide.** This document describes various aspects of the TMS320C5515 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.
- [SPRUGH5](#)— TMS320C5505 DSP System User's Guide.** This document describes various aspects of the TMS320C5505 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.
- [SPRUFX6](#)— TMS320C5514 DSP System User's Guide.** This document describes various aspects of the TMS320C5514 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

[SPRUGH6](#)— TMS320C5504 DSP System User's Guide. This document describes various aspects of the TMS320C5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

Real-Time Clock (RTC)

1.1 Introduction

This document describes features and operation of the real-time clock (RTC) on the TMS320C5515/14/05/04 Digital Signal Processor (DSP).

1.1.1 Purpose of the peripheral

The device includes a real time clock (RTC) that provides a time reference to an application executing on the DSP. The RTC has its own crystal input, clock domain, and core and I/O power supplies. The separate clock domain allows the RTC to run while the rest of the device is clock gated. All RTC registers are preserved and the counter continues to operate when the host CPU is clock gated. The RTC has the capability to wake-up the rest of the device through an alarm interrupt, periodic interrupt, or external WAKEUP signal.

1.1.2 Features

The real-time clock (RTC) provides the following features:

- RTC-only mode
- 100-year calendar up to year 2099.
- Counts milliseconds, seconds, minutes, hours, and date (including day, month, and year with leap year compensation).
- Millisecond time correction.
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm.
- 24-hour clock mode.
- Alarm interrupt for specific millisecond, second, minute, hour, day, month, and year.
- Periodic interrupt: every millisecond, second, minute, hour, or day.
- Single interrupt to the DSP CPU.
- 32.768kHz oscillator with frequency calibration.

The current date and time is tracked in a set of counter registers that update once per millisecond. The time is represented in 24-hour mode. For information on how to set the time and date, see [Section 1.2.4](#).

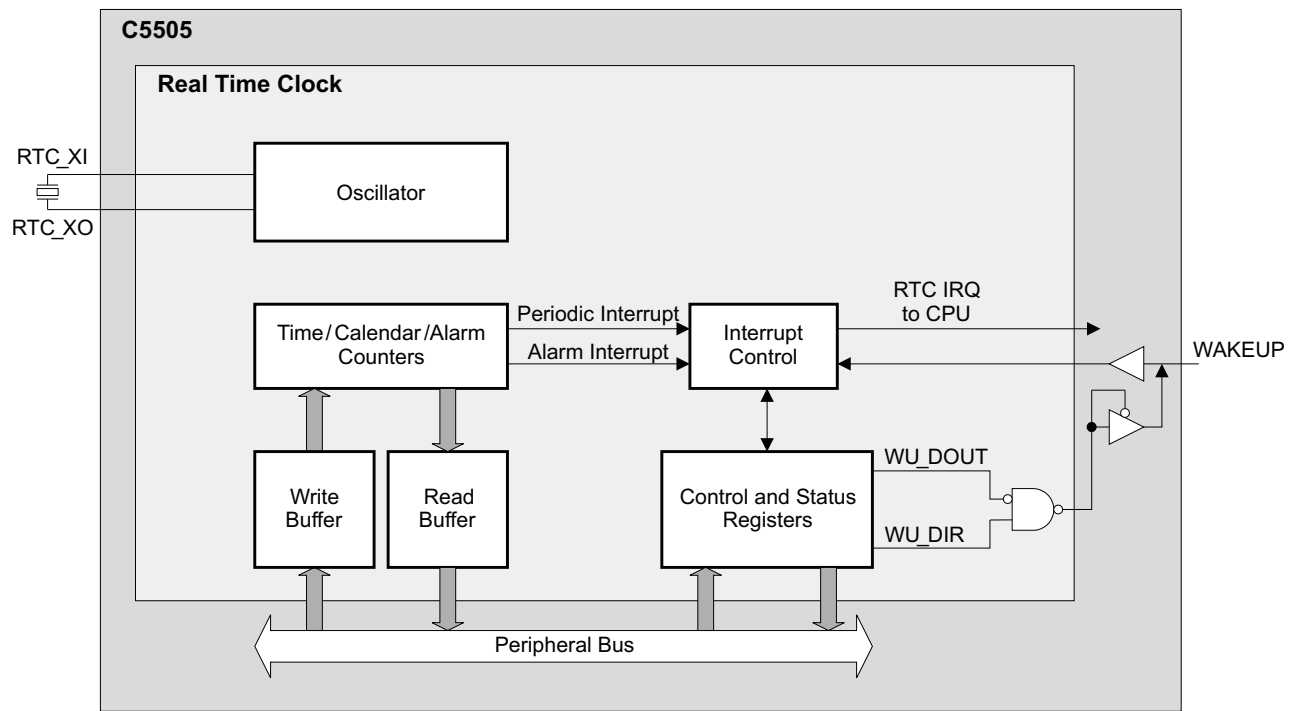
Alarms can be set to interrupt the DSP CPU at a particular time, or at periodic time intervals, such as once per minute or once per day. For information on how to set and use alarms, see [Section 1.2.5](#).

The clock reference for the RTC is an external 32.768kHz crystal (connected between signals RTC_XI and RTC_XO). The RTC also has separate core and I/O power supplies that are isolated from the rest of the DSP.

1.1.3 Functional Block Diagram

Figure 1-1 shows a block diagram of the RTC.

Figure 1-1. Block Diagram



1.2 Peripheral Architecture

This section describes the Real-Time Clock (RTC) Peripheral.

NOTE: If the RTC is not used, CV_{DDRTC} and DV_{DDRTC} must still be supplied because internal signals from the RTC are required for operation of the DSP's Power On Reset circuitry. In addition, the RTC_XI pin must be tied to CV_{DDRTC} and the RTC_XO pin must be tied to VSS. If the RTC_XI and RTC_XO pins are tied off, then the RTC registers are not accessible.

1.2.1 Clock Control

The RTC oscillator is driven by an external 32.768 KHz crystal connected between RTC_XI and RTC_XO

1.2.2 Signal Descriptions

As shown in Figure 1-1, the WAKEUP pin is a bidirectional pin that can be used as an input to wake-up the DSP clock domains or it can be used as an open-drain output to wake-up an external device. At power up the WAKEUP pin is configured as an input. This signal can be used to trigger the RTC interrupt to the CPU and to wake-up gated clocks regardless of whether the clocks were gated by the master clock gate or whether they were gated by the DSP's idle instruction.

When the WAKEUP pin is configured as an input ($RTCPMGT:WU_DIR = 0$), the RTC interrupt is enabled ($RTCINTEN: 0 = 1$) and the External Event Interrupt in $RTCINTREG$ is enabled ($RTCINTREG: EXTINTEN = 1$), a 0 to 1 transition on the WAKEUP pin will trigger the RTC interrupt. Additionally, when WAKEUP is high, then the Master Clock Gater for the whole digital core is forced into the un-gated state (clocks on). Note that the interrupt generation is edge sensitive while the clocks on condition is level sensitive. Please see Section 1.2.6 for Interrupt support.

1.2.3 RTC-Only Mode

RTC-only mode allows all supplies except DV_{DDRTC} and CV_{DDRTC} to be powered-down. In this mode, the RTC counter continues to operate. The RTC has the capability to wakeup the device from idle states via alarms, periodic interrupts, or an external WAKEUP input. Additionally, the RTC is able to output an alarm or periodic interrupt on the WAKEUP pin to cause external power management to re-enable power to the DSP core and I/O.

1.2.4 Using the Real-Time Clock Time and Calendar Registers

The current time and date are maintained in the RTC time and calendar registers. Information about how to use these registers is in the sections that follow.

1.2.4.1 Time/Calendar Data Format

The time and calendar data in the RTC is stored as binary-coded decimal (BCD) format. In BCD format, the decimal numbers 0 through 9 are encoded with their binary equivalent. Although most of the time/calendar registers have 4 bits assigned to each BCD digit, some of the register fields are shorter since the range of valid numbers may be limited. For example, only 3 bits are required to represent the first digit (most significant digit) of the “seconds” because only 0 through 5 are required.

The summary of the time/calendar registers is shown in [Table 1-1](#). The alarm registers are interleaved with the time/calendar registers and are not shown in this table. The alarm registers are shown in [Table 1-2](#). A complete description all RTC registers is available in [Section 1.3](#).

Table 1-1. Time/Calendar Registers

| Address (Hex) | Name | Function | Decimal Range | BCD Format |
|---------------|----------|-----------------------|---------------|------------|
| 1904h | RTCMIL | Milliseconds | 0-1023 | 0000-1023 |
| 1908h | RTCSEC | Seconds | 0-59 | 00-59 |
| 190Ch | RTCMIN | Minutes | 0-59 | 00-59 |
| 1910h | RTCHOUR | Hours (24) | 0-23 | 00-23 |
| 1914h | RTCDAY | Days | 1-31 | 01-31 |
| 1918h | RTCMONTH | Months (January = 01) | 1-12 | 01-12 |
| 191Ch | RTCYEAR | Years | 0-99 | 00-99 |

- The RTC Milliseconds Register (RTCMIL) stores the milliseconds value of the current time. After the milliseconds count reaches 1023 then the seconds register is updated by one. The reason for the rollover occurring at 1024, rather than 1000, is due to the crystal's oscillation frequency being a power of two, 32.768kHz. $32768 / 1024 = 32$ clocks per 'millisecond'. Thus, calling this register a 'milliseconds' register is a bit of a misnomer. The milliseconds digit 3 is 1 bit and the milliseconds digits 2:0 are 4 bits; digits 3:0 are encoded BCD values 0000 (0b 0000b 0000b 0000b) through 1023 (1b 0000b 0010b 0011b).
- The RTC Seconds Register (RTCSEC) stores the seconds value of the current time. The seconds digit 1 is 3 bits and the seconds digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 00 (000b 0000b) through 59 (101b 1001b).
- The RTC Minutes Register (RTCMIN) stores the minutes value of the current time. The minutes digit 1 is 3 bits and the minutes digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 00 (000b 0000b) through 59 (101b 1001b).
- The RTC Hours Register (RTCHOUR) stores the hours value of the current time. The hours digit 1 is 2 bits and the hours digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 01 (00b 0001b) through 23 (10b 0011b).
- The RTC Days Register (RTCDAY) stores the day of the month for the current date. The days digit 1 is 2 bits and the days digit 0 is 4 bits; digits 1 and 0 are encoded BCD 01 (00b 0001b) through 31 (11b 0001b).
- The RTC Months Register (RTCMONTH) stores the month for the current date. The months digit 1 is 1 bit and the months digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 01 (0b 0000b) through 12 (1b 0010b).

- The RTC Years Register (RTCYEAR) stores the year for the current date. The years digit 1 is 4 bits and the years digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 00 (0000b 0000b) through 99 (1001b 1001b).

1.2.4.2 Setting the Time/Calendar Register

The time/calendar registers are set or initialized by writing to the appropriate register bytes. To set date and time, write all the time and date registers. When written to, the data is stored to a buffer. Next, set the TIMEUPDT bit in the RTC Update Register (RTCUPDATE). Setting this bit causes the time/calendar values in the buffer to be loaded into the RTC simultaneously. All values should be encoded as BCD values.

1.2.4.3 Reading the Time/Calendar Registers

The time/calendar registers are updated every millisecond as the time changes. To get the most accurate time reading you should start with reading the Millisecond register (RTCMIL) and then the Second register (RTCSEC) followed by the remaining time/calendar register values (RTCMIN, RTCHOUR, RTCDAY, RTCMONTH, and RTCYEAR). Read the RTCMIL again and compare to the previous value. If both values are the same, an RTC update did not occur while the other registers were being read and all the values read represent the current time. If the Milliseconds have changed, this indicates that an RTC update occurred while the registers were being read and the process should be repeated. Results are unpredictable if values are written out of the register's normal range.

1.2.5 Using the Real-Time Clock Time and Calendar Alarms

Alarms can be configured to interrupt the CPU at a specific time, i.e., at specific values for the following:

- Milliseconds
- Seconds
- Minutes
- Hours
- Days of the month
- Months
- On specific Years

The time/calendar alarm registers control the setting of alarms. Information about how to use these registers can be found in the following sections. The alarms can be configured to generate an interrupt to the CPU or to wake-up the clocks. The operation of the alarm interrupt is described in [Section 1.2.6.4](#).

1.2.5.1 Time/Calendar Alarm Data Format

The time and calendar alarm data in the RTC is stored as binary-coded decimal (BCD) format. In BCD format, the decimal numbers 0 through 9 are encoded with their binary equivalent. Although most of the time/calendar alarm registers have 4 bits assigned to each BCD digit, some of the register field lengths may differ to accommodate the desired function.

The summary of the time/calendar alarm registers is shown in [Table 1-2](#). The time/calendar registers are interleaved with the alarm registers and are not shown in this table. The time/calendar registers are shown in [Table 1-1](#). A complete description of all RTC registers is available in [Section 1.3](#).

Table 1-2. Time and Calendar Alarm Data

| Address (Hex) | Name | Function | Decimal Range | BCD Format |
|---------------|-----------|-----------------------------|---------------|------------|
| 1905h | RTCMILA | Milliseconds alarm | 0-1023 | 0000-1023 |
| 1909h | RTCSECA | Seconds alarm | 0-59 | 00-59 |
| 190Dh | RTCMINA | Minutes alarm | 0-59 | 00-59 |
| 1911h | RTCHOURA | Hours (24) alarm | 0-23 | 00-23 |
| 1915h | RTCDAYA | Days alarm | 1-31 | 01-31 |
| 1919h | RTCMONTHA | Months (January = 01) alarm | 1-12 | 01-12 |

Table 1-2. Time and Calendar Alarm Data (continued)

| Address (Hex) | Name | Function | Decimal Range | BCD Format |
|---------------|----------|-------------|---------------|------------|
| 191Dh | RTCYEARA | Years alarm | 0-99 | 00-99 |

The RTC Milliseconds Alarm Register (RTCMILA) stores the milliseconds value of the desired alarm. The milliseconds alarm digit 3 is 1 bit and the milliseconds alarm digits 2:0 are 4; digits 3:0 are encoded BCD values 0000 (0b 0000b 0000b 0000b) through 1023 (1b 0000b 0010b 0011b). Values outside of the decimal range of 0 – 1023 will cause the alarm to never occur.

The RTC Seconds Alarm Register (RTCSECA) stores the seconds value of the desired alarm. The seconds alarm digit 1 is 3 bits and the seconds alarm digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 00 (000b 0000b) through 59 (101b 1001b). Values outside of the decimal range of 0 - 59 will cause the alarm to never occur.

The RTC Minutes Alarm Register (RTCMINA) stores the minute value of the desired alarm. The minutes alarm digit 1 is 3 bits and the minutes alarm digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 00 (000b 0000b) through 59 (101b 1001b). Values outside of the decimal range of 0 - 59 will cause the alarm to never occur.

The RTC Hours Alarm Register (RTCHOURA) stores the hour value of the desired alarm. The hours alarm digit 1 is 2 bits and the hours alarm digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 01 (00b 0001b) through 23 (10b 0011b). Values outside of the decimal range of 1 - 23 will cause the alarm to never occur.

The RTC Days Alarm Register (RTCDAYA) stores the day of the month value of the desired alarm. The days alarm digit 1 is 2 bits and the days alarm digit 0 is 4 bits; digits 1 and 0 are encoded BCD 01 (00b 0001b) through 31 (11b 0001b). Values outside of the decimal range of 1 - 31 will cause the alarm to never occur.

The RTC Months Alarm Register (RTCMONTHA) stores the month of the year value of the desired alarm. The months alarm digit 1 is 1 bit and the months alarm digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 01 (0b 0000b) through 12 (1b 0010b). Values outside the range 1 - 12 will cause the alarm to never occur.

The RTC Years Alarm Register (RTCYEARA) stores the year value of the desired alarm. The years alarm digit 1 is 4 bits and the years alarm digit 0 is 4 bits; digits 1 and 0 are encoded BCD values 00 (0000b 0000b) through 99 (1001b 1001b). Values outside the range 0 - 99 will cause the alarm to never occur.

1.2.5.2 Setting and reading the Time/Calendar Alarm Registers

The time/calendar alarm registers are set or initialized by writing to the appropriate register bytes. To set date and time, write all the time and date registers and then set the ALARMUPDT bit in the RTC Update Register (RTCUPDATE). This will simultaneously copy all the alarm register settings in one RTC cycle.

Time/calendar alarm registers can be read at any time and are not updated by the RTC.

1.2.5.3 Examples of Time/Calendar Alarm Settings

Some examples of various alarm settings are shown in [Table 1-3](#). A complete description of the RTC registers and their functions is provided in [Section 1.3](#).

Table 1-3. Time/Calendar Alarm Settings

| Alarm Occurs... | RTCYEARA | RTCMONTHA | RTCDAYA | RTCHOURA | RTCMINA | RTCSECA | RTCMILA |
|-------------------------------------|----------|-----------|---------|----------|---------|---------|---------|
| May 7, 2010 @ 3:19:46 AM | 10h | 5h | 7h | 3h | 19h | 46h | 0h |
| Dec 22, 2099 @ 5:50:15 and 300ms PM | 99h | 12h | 22h | 17h | 50h | 15h | 300h |

1.2.6 Real-Time Clock Interrupt Requests

The RTC provides the ability to interrupt the CPU based on three events: a periodic interrupt, an alarm interrupt, or an external "Wakeup" interrupt. Although three interrupt sources are available, the RTC makes a single interrupt request to the CPU. Specific information about using each of the interrupt types is in the sections that follow.

1.2.6.1 Interrupt Enable

The RTC has two registers for enabling interrupts. The RTC Interrupt Enable (RTCINTEN) enables the RTC interrupt to the CPU. This bit allows any interrupt that is triggered in the RTC to be sent to the CPU. The second register is the RTC Interrupt Register (RTSINTREG) is used to enable the different interrupt events that can be passed to the CPU. These include the following:

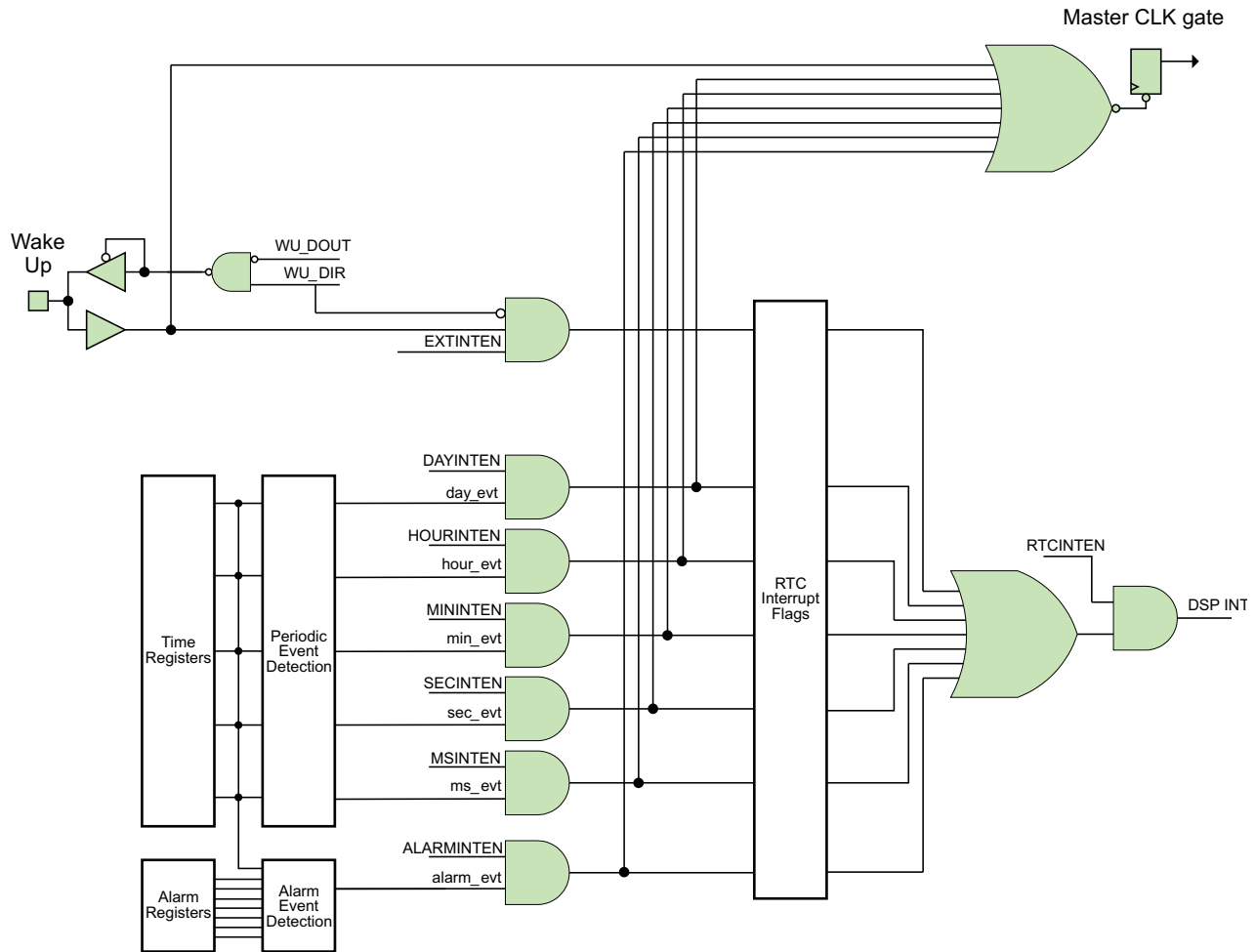
- Alarm Interrupt
- External "wakeup" Interrupt
- Periodic Day Interrupt
- Periodic Hour Interrupt
- Periodic Minute Interrupt
- Periodic Second Interrupt
- Periodic Millisecond Interrupt

NOTE: To use the external wakeup interrupt, you must set the WU_DIR bit in the RTCPMGT register to 0.

When a RTC interrupt is generated, the RTC's interrupt is directed to two places (see [Figure 1-2](#)).

1. System Clock Wakeup Logic – the interrupt will cause the Master Clock Gater to enable the Master Clock.
2. The RTC interrupt can be directed to the CPU if RTCINTEN = 1. The CPU's RTC interrupt must be unmasked for the CPU to respond to the interrupt.
 - If the CPU is idled, the interrupt will cause the CPU to exit idle. If interrupts are globally enabled, the CPU will execute the RTC ISR.
 - If the CPU is not idled and interrupts are globally enabled, the CPU will execute the RTC ISR.

Figure 1-2. RTC Interrupt and Wakeup Logic



1.2.6.2 Interrupt Flag Bits

When the interrupts are enabled in [Section 1.2.6.1](#) and the event occurs, the equivalent flag is set in the RTC Interrupt Flag Register (RTCINTFL). See [Section 1.3](#) for complete details of the RTC registers. The flagged event is cleared when the programmer writes a "1" to the flag bit.

There is also an RTC Lost Power Register (RTCNOPWR). If this flag is set the RTC has lost power and requires a software reset. NOTE: at least 3 RTC clock cycles must elapse after power-up in order to read valid data since the synchronization logic between the CPU and RTC consumes 3 RTC clock cycles.

If the RTC Interrupt enable bit is set and any of the active events occur then an RTC interrupt is sent to the CPU. The RTC interrupt is asserted as long as at least one of the interrupt flag bits is set. When an interrupt occurs from the RTC, the source of the interrupt can be determined by reading the flag bits in RTCINTFL.

1.2.6.3 Periodic Interrupt Request

Periodic Interrupts cause the RTC to make an interrupt request to the CPU periodically. The periodicity can be every millisecond, every second, every minute, hourly, or daily. The periodic interrupt rate is selected using the RTC Interrupts Register (RTCINTREG), see [Table 1-4](#). Writing a 1 to these bits enables the periodic interrupt. Writing a 0 disables the interrupt. Once the interrupt occurs it will remain active until the corresponding flag bit in the RTC Status Register is cleared.

NOTE: The interrupt occurs whenever that particular time value is incremented.

Table 1-4. Periodic Interrupts

| RTCINTREG bits | Periodic interrupt rate |
|----------------|-------------------------|
| Bit 0 | Every Millisecond |
| Bit 1 | Every Second |
| Bit 2 | Every Minute |
| Bit 3 | Every Hour |
| Bit 4 | Every Day |

To use the RTC Periodic interrupt:

- Select the desired interrupt period by enabling the proper interrupt in the RTCINTREG
- Enable the RTC interrupt to the CPU by setting bit 0 of RTCINTEN

When the periodic interrupt occurs, the corresponding interrupt flag will be set in the RTC Interrupt Flag (RTCINTFL) register and the interrupt is sent to the CPU.

1.2.6.4 Alarm Interrupt Request

The RTC alarm interrupt can be used to generate an interrupt to the CPU at a specific time. The alarm interrupt occurs when the alarm time programmed in the RTC alarm registers match the current time. For information about programming an alarm time, see [Section 1.2.5](#).

To use the RTC alarm interrupt:

- Select the desired alarm time by configuring the RTC alarm registers.
- Enable the RTC alarm interrupt by setting bit 15 of the RTCINTREG.
- Enable the RTC interrupt to the CPU by setting bit 0 of RTCINTEN

When the alarm interrupt occurs, the Alarm Flag (bit 15) in the RTCINTFL register will be set and the RTC interrupt is sent to the CPU.

1.2.6.5 WAKEUP Interrupt Request

The external WAKEUP signal or RTC alarm trigger sends a WAKEUP event to the System Clock Wakeup Logic. This asynchronously clears the clock gate which gates the Master Clock, and enables the Master Clock. When the DSP wakes up due to an RTC alarm, periodic interrupt, or by the external WAKEUP signal, the DSP latches the RTC interrupt. Because there is only one interrupt line for the RTC, the user must look at the RTC status register to determine which RTC event caused the wake-up.

1.2.7 Reset Considerations

The RTC can be reset by the RTCRESET bit located in the RTC oscillator register (RTCOSC). The RTC can also be reset by an internal POR circuit that monitors VDD_RTC. Neither the RESETN pin nor the DSP's POR can reset the RTC.

1.2.7.1 Software Reset Considerations

The DSP can cause a software reset of the RTC when the RTCRESET bit is set to 1. When this occurs, all RTC registers are reset to the default settings. The RTC will not be reset when the RESETN pin goes low. After a RTC software reset, do not access any RTC register for three 32.768kHz clock cycles after setting the software reset bit.

1.2.7.2 Hardware Reset Considerations

The RTC has a hardware reset that is tied to a POR circuit that monitors the VDD_RTC. The RTC is not reset with the RESETN pin or the DSP's POR.

1.3 Registers

This section describes the memory-mapped registers for the Real Time Clock (RTC).

Control of the RTC is maintained through a set of I/O memory mapped registers shown in [Table 1-5](#). The first two registers in Table 5, RTCINTEN and RTCUPDATE, are located in the DSP core power domain, while the remaining registers in Table 5 are located in the RTC power domain. Writes to registers in the RTC power domain are synchronized to the RTC 32.768 kHz clock and can therefore take many CPU clock cycles to complete. The CPU clock must run at least 3X faster than the RTC, and writes to registers in the RTC domain will not be evident for up to two 32.768kHz clock cycles. If the RTC Oscillator is disabled (RTC_XI and RTC_XO pins tied off), no RTC register in the RTC power domain can be written.

Table 1-5. Real Time Clock (RTC) Registers

| CPU Word Address | Acronym | Register Description | Section |
|------------------|-----------|--------------------------------|--------------------------------|
| 1900h | RTCINTEN | RTC Interrupt Enable Register | Section 1.3.1 |
| 1901h | RTCUPDATE | RTC Update Register | Section 1.3.2 |
| 1904h | RTCMIL | Milliseconds Register | Section 1.3.3 |
| 1905h | RTCMILA | Milliseconds Alarm Register | Section 1.3.4 |
| 1908h | RTCSEC | Seconds Register | Section 1.3.5 |
| 1909h | RTCSECA | Seconds Alarm Register | Section 1.3.6 |
| 190Ch | RTCMIN | Minutes Register | Section 1.3.7 |
| 190Dh | RTCMINA | Minutes Alarm Register | Section 1.3.8 |
| 1910h | RTCHOUR | Hours Register | Section 1.3.9 |
| 1911h | RTCHOURA | Hours Alarm Register | Section 1.3.10 |
| 1914h | RTCDAY | Days Register | Section 1.3.11 |
| 1915h | RTCDAYA | Days Alarm Register | Section 1.3.12 |
| 1918h | RTCMONTH | Months Register | Section 1.3.13 |
| 1919h | RTCMONTHA | Months Alarm Register | Section 1.3.14 |
| 191Ch | RTCYEAR | Years Register | Section 1.3.15 |
| 191Dh | RTCYEARA | Years Alarm Register | Section 1.3.16 |
| 1920h | RTCINTFL | RTC Interrupt Flag Register | Section 1.3.17 |
| 1921h | RTCNOPWR | RTC Lost Power Status Register | Section 1.3.18 |
| 1924h | RTCINTREG | RTC Interrupt Register | Section 1.3.19 |
| 1928h | RTCDRIFT | RTC Compensation Register | Section 1.3.20 |
| 192Ch | RTCOSC | RTC Oscillator Register | Section 1.3.21 |
| 1930h | RTCPMGT | RTC Power Management Register | Section 1.3.22 |
| 1960h | RTCSCR1 | RTC LSW Scratch Register 1 | Section 1.3.23 |
| 1961h | RTCSCR2 | RTC MSW Scratch Register 2 | Section 1.3.24 |
| 1964h | RTCSCR3 | RTC LSW Scratch Register 3 | Section 1.3.25 |
| 1965h | RTCSCR4 | RTC MSW Scratch Register 4 | Section 1.3.26 |

1.3.1 RTC Interrupt Enable Register (RTCINTEN)

The RTC interrupt enable register (RTCINTEN) is shown in [Figure 1-3](#) and described in [Table 1-6](#).

Figure 1-3. RTC Interrupt Enable Register (RTCINTEN)

| | | |
|----------|---|----------|
| 15 | 1 | 0 |
| Reserved | | RTCINTEN |
| R-0 | | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-6. RTC Interrupt Enable Register (RTCINTEN) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|----------------------------|
| 15-1 | Reserved | 0 | Reserved. |
| 0 | RTCINTEN | 0 | RTC interrupt enable. |
| | | 0 | RTC interrupt is disabled. |
| | | 1 | RTC interrupt is enabled. |

1.3.2 RTC Update Register (RTCUPDATE)

The RTC update register (RTCUPDATE) is shown in [Figure 1-4](#) and described in [Table 1-7](#).

Figure 1-4. RTC Update Register (RTCUPDATE)

| | | | |
|----------|-----------|----------|---|
| 15 | 14 | 13 | 0 |
| TIMEUPDT | ALARMUPDT | Reserved | |
| RW-0 | RW-0 | R-0 | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-7. RTC Update Register (RTCUPDATE) Field Descriptions

| Bit | Field | Value | Description |
|------|-----------|-------|---|
| 15 | TIMEUPDT | 0 | Initiates the Time updates. |
| | | 0 | RTC time registers updated. |
| | | 1 | Initiates the transfer of the time registers from the DSP to the RTC. |
| 14 | ALARMUPDT | 0 | Initiates the alarm updates. |
| | | 0 | RTC alarm registers updated. |
| | | 1 | Initiate update of the alarm registers. |
| 13-0 | Reserved | 0 | Reserved. |

1.3.3 Milliseconds Register (RTCMIL)

The milliseconds register (RTCMIL) is shown in [Figure 1-5](#) and described in [Table 1-8](#).

Figure 1-5. Milliseconds Register (RTCMIL)

| | | | | | | | | |
|----------|------|------|------|------|---|---|---|---|
| 15 | 13 | 12 | 11 | 8 | 7 | 4 | 3 | 0 |
| Reserved | MS3 | MS2 | MS1 | MS0 | | | | |
| R-0 | RW-0 | RW-0 | RW-0 | RW-0 | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-8. Milliseconds Register (RTCMIL) Field Descriptions

| Bit | Field | Value | Description |
|-------|----------|--------|--|
| 15-13 | Reserved | 0 | Reserved. |
| 12 | MS3 | 0 1 | Digit 3 of Milliseconds in BCD format. Digit 3 of MS is 0. Digit 3 of MS is 1. |
| 11-8 | MS2 | 0-9 | Digit 2 of Milliseconds in BCD format. |
| 7-4 | MS1 | 0-9 | Digit 1 of Milliseconds in BCD format. |
| 3-0 | MS0 | 0-9 | Digit 0 of Milliseconds in BCD format. |

1.3.4 Milliseconds Alarm Register (RTCMILA)

The milliseconds alarm register (RTCMILA) is shown in [Figure 1-6](#) and described in [Table 1-9](#).

Figure 1-6. Milliseconds Alarm Register (RTCMILA)

| | | | | | | | | |
|----------|------|------|------|------|---|---|---|---|
| 15 | 13 | 12 | 11 | 8 | 7 | 4 | 3 | 0 |
| Reserved | MSA3 | MSA2 | MSA1 | MSA0 | | | | |
| R-0 | RW-0 | RW-0 | RW-0 | RW-0 | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

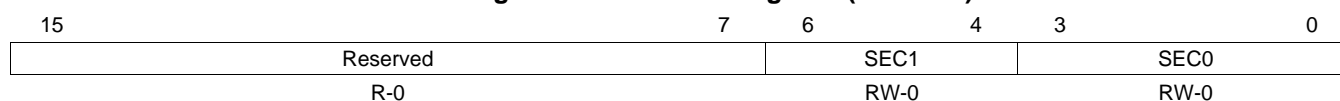
Table 1-9. Milliseconds Alarm Register (RTCMILA) Field Descriptions

| Bit | Field | Value | Description |
|-------|----------|--------|---|
| 15-13 | Reserved | 0 | Reserved. |
| 12 | MSA3 | 0 1 | Digit 3 of Millisecond alarm in BCD format. Digit 3 of MS Alarm is 0. Digit 3 of MS Alarm is 1. |
| 11-8 | MSA2 | 0-9 | Digit 2 of Millisecond alarm in BCD format. |
| 7-4 | MSA1 | 0-9 | Digit 1 of Millisecond alarm in BCD format. |
| 3-0 | MSA0 | 0-9 | Digit 0 of Millisecond alarm in BCD format. |

1.3.5 Seconds Register (RTCSEC)

The seconds register (RTCSEC) is shown in [Figure 1-7](#) and described in [Table 1-10](#).

Figure 1-7. Seconds Register (RTCSEC)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

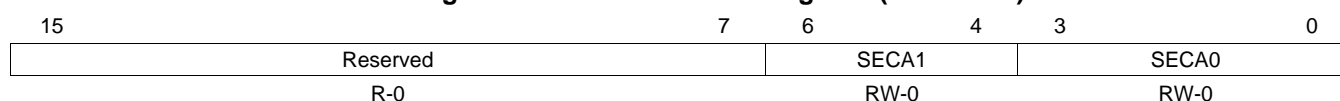
Table 1-10. Seconds Register (RTCSEC) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|-----------------------------------|
| 15-7 | Reserved | 0 | Reserved. |
| 6-4 | SEC1 | 0-5 | Digit 1 of Seconds in BCD format. |
| 3-0 | SEC0 | 0-9 | Digit 0 of Seconds in BCD format. |

1.3.6 Seconds Alarm Register (RTCSECA)

The seconds alarm register (RTCSECA) is shown in [Figure 1-8](#) and described in [Table 1-11](#).

Figure 1-8. Seconds Alarm Register (RTCSECA)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-11. Seconds Alarm Register (RTCSECA) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|---|
| 15-7 | Reserved | 0 | Reserved. |
| 6-4 | SECA1 | 0-5 | Digit 1 of Seconds Alarm in BCD format. |
| 3-0 | SECA0 | 0-9 | Digit 0 of Seconds Alarm in BCD format. |

1.3.7 Minutes Register (RTCMIN)

The minutes register (RTCMIN) is shown in [Figure 1-9](#) and described in [Table 1-12](#).

Figure 1-9. Minutes Register (RTCMIN)

| | | | | | |
|----------|---|---|------|------|---|
| 15 | 7 | 6 | 4 | 3 | 0 |
| | | | | | |
| Reserved | | | MIN1 | MIN0 | |
| R-0 | | | RW-0 | RW-0 | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-12. Minutes Register (RTCMIN) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|-----------------------------------|
| 15-7 | Reserved | 0 | Reserved. |
| 6-4 | MIN1 | 0-5 | Digit 1 of Minutes in BCD format. |
| 3-0 | MIN0 | 0-9 | Digit 0 of Minutes in BCD format. |

1.3.8 Minutes Alarm Register (RTCMINA)

The minutes alarm register (RTCMINA) is shown in [Figure 1-10](#) and described in [Table 1-13](#).

Figure 1-10. Minutes Alarm Register (RTCMINA)

| | | | | | |
|----------|---|---|-------|-------|---|
| 15 | 7 | 6 | 4 | 3 | 0 |
| | | | | | |
| Reserved | | | MINA1 | MINA0 | |
| R-0 | | | RW-0 | RW-0 | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-13. Minutes Alarm Register (RTCMINA) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|---|
| 15-7 | Reserved | 0 | Reserved. |
| 6-4 | MINA1 | 0-5 | Digit 1 of Minutes Alarm in BCD format. |
| 3-0 | MINA0 | 0-9 | Digit 0 of Minutes Alarm in BCD format. |

1.3.9 Hours Register (RTCHOUR)

The hours register (RTCHOUR) is shown in [Figure 1-11](#) and described in [Table 1-14](#).

Figure 1-11. Hours Register (RTCHOUR)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

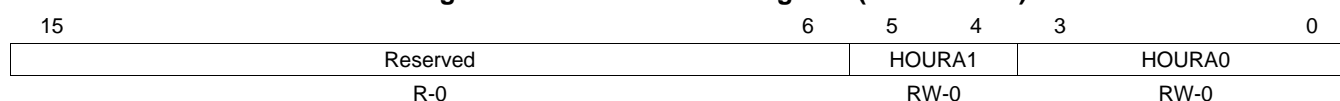
Table 1-14. Hours Register (RTCHOUR) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|---------------------------------|
| 15-6 | Reserved | 0 | Reserved. |
| 5-4 | HOUR1 | 0-2 | Digit 1 of Hours in BCD format. |
| 3-0 | HOUR0 | 0-9 | Digit 0 of Hours in BCD format. |

1.3.10 Hours Alarm Register (RTCHOURA)

The hours alarm register (RTCHOURA) is shown in [Figure 1-12](#) and described in [Table 1-15](#).

Figure 1-12. Hours Alarm Register (RTCHOURA)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-15. Hours Alarm Register (RTCHOURA) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|---------------------------------------|
| 15-6 | Reserved | 0 | Reserved. |
| 5-4 | HOURA1 | 0-2 | Digit 1 of Hours Alarm in BCD format. |
| 3-0 | HOURA0 | 0-9 | Digit 0 of Hours Alarm in BCD format. |

1.3.11 Days Register (RTCDAY)

The days register (RTCDAY) is shown in [Figure 1-13](#) and described in [Table 1-16](#).

Figure 1-13. Days Register (RTCDAY)

| | | | | | | | |
|----------|--|---|---|---|---|------|------|
| 15 | | 6 | 5 | 4 | 3 | | 0 |
| Reserved | | | | | | DAY1 | DAY0 |
| R-0 | | | | | | RW-0 | RW-1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-16. Days Register (RTCDAY) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|--------------------------------|
| 15-6 | Reserved | 0 | Reserved. |
| 5-4 | DAY1 | 0-3 | Digit 1 of Days in BCD format. |
| 3-0 | DAY0 | 0-9 | Digit 0 of Days in BCD format. |

1.3.12 Days Alarm Register (RTCDAYA)

The days alarm register (RTCDAYA) is shown in [Figure 1-14](#) and described in [Table 1-17](#).

Figure 1-14. Days Alarm Register (RTCDAYA)

| | | | | | | | |
|----------|--|---|---|---|---|-------|-------|
| 15 | | 6 | 5 | 4 | 3 | | 0 |
| Reserved | | | | | | DAYA1 | DAYA0 |
| R-0 | | | | | | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-17. Days Alarm Register (RTCDAYA) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|--------------------------------------|
| 15-6 | Reserved | 0 | Reserved. |
| 5-4 | DAYA1 | 0-3 | Digit 1 of Days Alarm in BCD format. |
| 3-0 | DAYA0 | 0-9 | Digit 0 of Days Alarm in BCD format. |

1.3.13 Months Register (RTCMONTH)

The months register (RTCMONTH) is shown in [Figure 1-15](#) and described in [Table 1-18](#).

Figure 1-15. Months Register (RTCMONTH)

| | | | | |
|----------|---|---|--------|--------|
| 15 | 5 | 4 | 3 | 0 |
| | | | | |
| Reserved | | | MONTH1 | MONTH0 |
| R-0 | | | RW-0 | RW-1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-18. Months Register (RTCMONTH) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|----------------------------------|
| 15-5 | Reserved | 0 | Reserved. |
| 4 | MONTH1 | 0-1 | Digit 1 of Months in BCD format. |
| 3-0 | MONTH0 | 0-9 | Digit 0 of Months in BCD format. |

1.3.14 Months Alarm Register (RTCMONTHA)

The months alarm register (RTCMONTHA) is shown in [Figure 1-16](#) and described in [Table 1-19](#).

Figure 1-16. Months Alarm Register (RTCMONTHA)

| | | | | |
|----------|---|---|---------|---------|
| 15 | 5 | 4 | 3 | 0 |
| | | | | |
| Reserved | | | MONTHA1 | MONTHA0 |
| R-0 | | | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

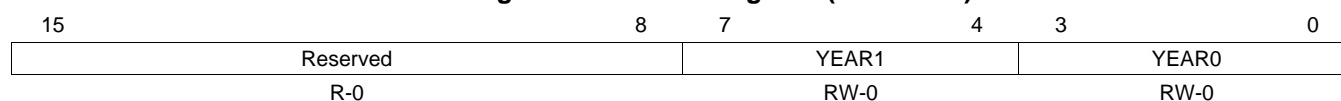
Table 1-19. Months Alarm Register (RTCMONTHA) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|--|
| 15-5 | Reserved | 0 | Reserved. |
| 4 | MONTHA1 | 0-1 | Digit 1 of Months Alarm in BCD format. |
| 3-0 | MONTHA0 | 0-9 | Digit 0 of Months Alarm in BCD format. |

1.3.15 Years Register (RTCYEAR)

The years register (RTCYEAR) is shown in [Figure 1-17](#) and described in [Table 1-20](#).

Figure 1-17. Years Register (RTCYEAR)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

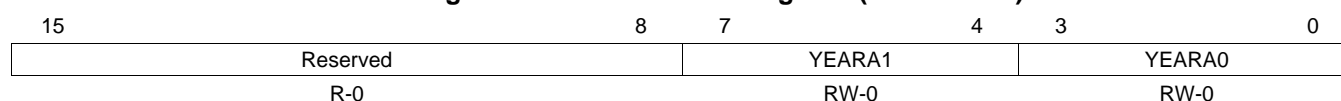
Table 1-20. Years Register (RTCYEAR) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|---------------------------------------|
| 15-8 | Reserved | 0 | Reserved. |
| 7-4 | YEAR1 | 0-9 | Digit 1 of Year in BCD format (20XX). |
| 3-0 | YEAR0 | 0-9 | Digit 0 of Year in BCD format (20XX). |

1.3.16 Years Alarm Register (RTCYEARA)

The years alarm register (RTCYEARA) is shown in [Figure 1-18](#) and described in [Table 1-21](#).

Figure 1-18. Years Alarm Register (RTCYEARA)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-21. Years Alarm Register (RTCYEARA) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|---|
| 15-8 | Reserved | 0 | Reserved. |
| 7-4 | YEARA1 | 0-9 | Digit 1 of Year Alarm in BCD format (20XX). |
| 3-0 | YEARA0 | 0-9 | Digit 0 of Year Alarm in BCD format (20XX). |

1.3.17 RTC Interrupt Flag Register (RTCINTFL)

The RTC interrupt flag register (RTCINTFL) is shown in [Figure 1-19](#) and described in [Table 1-22](#).

Figure 1-19. RTC Interrupt Flag Register (RTCINTFL)

| | | | | | | | | | | | | | | | |
|----------|--|----------|--|-------|--|-------|---|--------|--|-------|--|-------|--|-------|--|
| 15 | | 14 | | | | | 8 | | | | | | | | |
| ALARMFL | | Reserved | | | | | | | | | | | | | |
| R/W-0 | | R-0 | | | | | | | | | | | | | |
| 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | 0 | |
| Reserved | | | | EXTFL | | DAYFL | | HOURFL | | MINFL | | SECFL | | MSFL | |
| R-0 | | | | R/W-0 | | R/W-0 | | R/W-0 | | R/W-0 | | R/W-0 | | R/W-0 | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-22. RTC Interrupt Flag Register (RTCINTFL) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|--------|--|
| 15 | ALARMFL | 0 1 | Flag indicating whether an Alarm interrupt has occurred. Alarm interrupt did not occur. Alarm interrupt occurred (write 1 to clear). |
| 14-6 | Reserved | 0 | Reserved. |
| 5 | EXTFL | 0 1 | Flag indicating whether an external event interrupt (WAKEUP pin) has occurred. External event interrupt did not occur. External event interrupt occurred (write 1 to clear). |
| 4 | DAYFL | 0 1 | Flag indicating whether a periodic Day interrupt has occurred. Periodic Day interrupt did not occur. Periodic Day interrupt occurred (write 1 to clear). |
| 3 | HOURFL | 0 1 | Flag indicating whether a periodic Hour event interrupt has occurred. Periodic Hour interrupt did not occur. Periodic Hour interrupt occurred (write 1 to clear). |
| 2 | MINFL | 0 1 | Flag indicating whether a periodic Minute event interrupt has occurred. Periodic Minute interrupt did not occur. Periodic Minute interrupt occurred (write 1 to clear). |
| 1 | SECFL | 0 1 | Flag indicating whether a periodic Second event interrupt has occurred. Periodic Second interrupt did not occur. Periodic Second interrupt occurred (write 1 to clear). |
| 0 | MSFL | 0 1 | Flag indicating whether a periodic Millisecond event interrupt has occurred. Periodic Millisecond interrupt did not occur. Periodic Millisecond interrupt occurred (write 1 to clear). |

1.3.18 RTC Lost Power Status Register (RTCNOPWR)

The RTC lost power status register (RTCNOPWR) is shown in [Figure 1-20](#) and described in [Table 1-23](#).

Figure 1-20. RTC Lost Power Status Register (RTCNOPWR)

| | | | |
|----------|--|---|-------|
| 15 | | 1 | 0 |
| Reserved | | | PWRUP |
| R-0 | | | R-1 |

LEGEND: R = Read only; -n = value after reset

Table 1-23. RTC Lost Power Status Register (RTCNOPWR) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|-------|---|
| 15-1 | Reserved | 0 | Reserved. |
| 0 | PWRUP | 0 | RTC has lost power Flag. |
| | | 0 | RTC has not lost power since software reset. |
| | | 1 | RTC has lost power and requires a software reset and initialization of the time registers to the current time and date. |
| | | | PWRUP is cleared by a read of RTCINTFL or RTCNOPWR. Therefore, read RTCNOPWR before reading RTCINTFL to obtain the correct PWRUP value. |

1.3.19 RTC Interrupt Register (RTCINTREG)

The RTC interrupt register (RTCINTREG) is shown in [Figure 1-21](#) and described in [Table 1-24](#).

Figure 1-21. RTC Interrupt Register (RTCINTREG)

| | | | | | | | | |
|------------|--|----------|----------|-----------|----------|----------|---------|---|
| 15 | | 14 | | | | | 8 | |
| ALARMINTEN | | Reserved | | | | | | |
| R/W-0 | | R-0 | | | | | | |
| 7 | | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | EXTINTEN | DAYINTEN | HOURINTEN | MININTEN | SECINTEN | MSINTEN | |
| R-0 | | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-24. RTC Interrupt Register (RTCINTREG) Field Descriptions

| Bit | Field | Value | Description |
|------|------------|--------|--|
| 15 | ALARMINTEN | 0 1 | Alarm interrupt enable. Alarm interrupt not enabled. Alarm interrupt enabled. |
| 14-6 | Reserved | 0 | Reserved. |
| 5 | EXTINTEN | 0 1 | External event (WAKEUP pin) interrupt enable. External event interrupt not enabled. External event interrupt enabled. |
| 4 | DAYINTEN | 0 1 | Periodic Day interrupt enable. Periodic Day interrupt not enabled. Periodic Day interrupt enabled. |
| 3 | HOURINTEN | 0 1 | Periodic Hour interrupt enable. Periodic Hour interrupt not enabled. Periodic Hour interrupt enabled. |
| 2 | MININTEN | 0 1 | Periodic Minute interrupt enable. Periodic Minute interrupt not enabled. Periodic Minute interrupt enabled. |
| 1 | SECINTEN | 0 1 | Periodic Second interrupt enable. Periodic Second interrupt not enabled. Periodic Second interrupt enabled. |
| 0 | MSINTEN | 0 1 | Periodic Millisecond interrupt enable. Periodic Millisecond interrupt not enabled. Periodic Millisecond interrupt enabled. |

1.3.20 RTC Compensation Register (RTCDRIFT)

Every hour on the hour, a positive or negative number of milliseconds is added to the milliseconds register to compensate for inaccuracy in the 32.768kHz crystal based on the value of COMP[3:0]. If this value is 0 then no compensation will be applied.

NOTE: Any positive compensation value must not be a multiple of 10.

The RTC compensation register (RTCDRIFT) is shown in [Figure 1-22](#) and described in [Table 1-25](#).

Figure 1-22. RTC Compensation Register (RTCDRIFT)

| | | | | | | | | | |
|-------|----------|-------|-------|-------|-------|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 8 | 7 | 4 | 3 | 0 |
| DRIFT | Reserved | COMP3 | COMP2 | COMP1 | COMP0 | | | | |
| RW-0 | R-0 | RW-0 | RW-0 | RW-0 | RW-0 | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-25. RTC Compensation Register (RTCDRIFT) Field Descriptions

| Bit | Field | Value | Description |
|-------|----------|--------|--|
| 15 | DRIFT | 0 1 | Positive or Negative Compensation. Negative compensation. Positive compensation. |
| 14-13 | Reserved | 0 | Reserved. |
| 12 | COMP3 | 0 1 | Digit 3 of Compensation in BCD format. Digit 3 of Compensation is 0. Digit 3 of Compensation is 1. |
| 11-8 | COMP2 | 0-9 | Digit 2 of Compensation register in BCD format. |
| 7-4 | COMP1 | 0-9 | Digit 1 of Compensation register in BCD format. |
| 3-0 | COMP0 | 0-9 | Digit 0 of Compensation register in BCD format. |

1.3.21 RTC Oscillator Register (RTCOSC)

The RTC oscillator register (RTCOSC) is shown in [Figure 1-23](#) and described in [Table 1-26](#).

Figure 1-23. RTC Oscillator Register (RTCOSC)

| | | | | |
|----------|----------|----------|---|---|
| 15 | 14 | 4 | 3 | 0 |
| RTCRESET | Reserved | OSCRES | | |
| W-0 | R-0 | RW-1011b | | |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; n = value after reset

Table 1-26. RTC Oscillator Register (RTCOSC) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|--------|---|
| 15 | RTCRESET | 0 1 | RTC software reset. The RTC only resets when this bit is set. The RTC is not reset when RESTN goes low. Once set, this bit is cleared by the RTC. Do not access any RTC register for three 32.768kHz clock cycles after setting this bit. RTC not reset. RTC reset. |
| 14-4 | Reserved | 0 | Reserved. |
| 3-0 | OSCRES | 0-Fh | Value of the oscillator cell's internal resistor. The default (reset state) is 1011b and this gives faster startup but higher power. Once the oscillator is running it can be changed to 1000b for lower power consumption. |

1.3.22 RTC Power Management Register (RTCPMGT)

The RTC power management register (RTCPMGT) is shown in [Figure 1-24](#) and described in [Table 1-27](#).

Figure 1-24. RTC Power Management Register (RTCPMGT)

| | | | | | | |
|----------|---|---------|--------|-------|--------|-------------|
| 15 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | WU_DOUT | WU_DIR | BG_PD | LDO_PD | RTCCLKOUTEN |
| R-0 | | RW-1 | RW-0 | RW-0 | RW-0 | RW-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-27. RTC Power Management Register (RTCPMGT) Field Descriptions

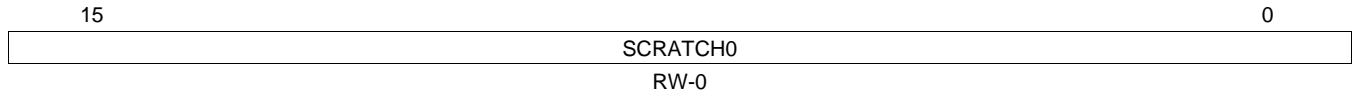
| Bit | Field | Value | Description |
|------|-------------|-------|--|
| 15-5 | Reserved | 0 | Reserved. |
| 4 | WU_DOUT | 0 | Wake-up output, active low/open-drain. WAKEUP pin driven low. |
| | | 1 | WAKEUP pin is in high impedance. |
| 3 | WU_DIR | 0 | Wake-up pin direction control. WAKEUP pin is configured as input. |
| | | 1 | WAKEUP pin is configured as output. Note: The WAKEUP pin, when configured as an input, is active high. When it is configured as an output, it is open-drain and thus it should have an external pullup and it is active low. |
| 2 | BG_PD | 0 | [Not supported on this device. Reserved for compatibility with future devices]. Bandgap power down. Normal. |
| | | 1 | Reserved. |
| 1 | LDO_PD | 0 | [Not supported on this device. Reserved for compatibility with future devices]. LDO power down. Normal. |
| | | 1 | Reserved. |
| 0 | RTCCLKOUTEN | 0 | Clockout output enable. RTC clock output disabled. |
| | | 1 | RTC clock output enabled. |

1.3.23 RTC LSW Scratch Register 1 (RTCSCR1)

The RTC Scratch Registers are general purpose memory that can be used to store a value that will be preserved even when the DSP power is off.

The RTC LSW scratch register 1 (RTCSCR1) is shown in [Figure 1-25](#) and described in [Table 1-28](#).

Figure 1-25. RTC LSW Scratch Register 1 (RTCSCR1)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

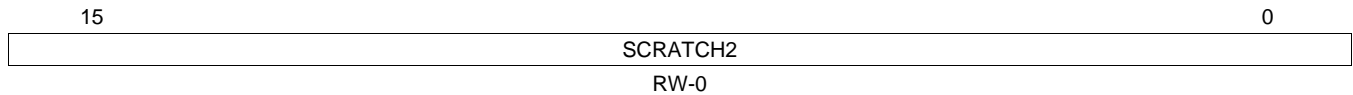
Table 1-28. RTC LSW Scratch Register 1 (RTCSCR1) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|---------|--|
| 15-0 | SCRATCH0 | 0-FFFFh | Scratch registers, available to program. |

1.3.24 RTC MSW Scratch Register 2 (RTCSCR2)

The RTC MSW scratch register 2 (RTCSCR2) is shown in [Figure 1-26](#) and described in [Table 1-29](#).

Figure 1-26. RTC MSW Scratch Register 2 (RTCSCR2)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

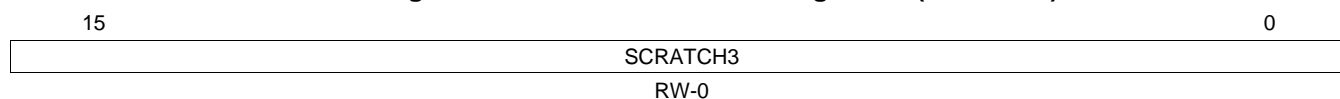
Table 1-29. RTC MSW Scratch Register 2 (RTCSCR2) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|---------|--|
| 15-0 | SCRATCH2 | 0-FFFFh | Scratch registers, available to program. |

1.3.25 RTC LSW Scratch Register 3 (RTCSCR3)

The RTC LSW scratch register 3 (RTCSCR3) is shown in [Figure 1-27](#) and described in [Table 1-30](#).

Figure 1-27. RTC LSW Scratch Register 3 (RTCSCR3)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

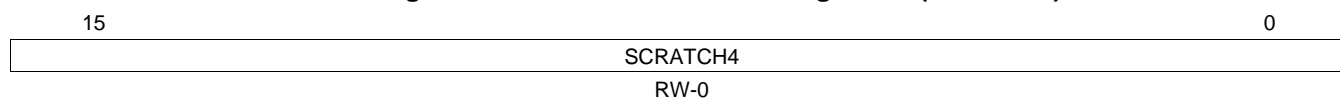
Table 1-30. RTC LSW Scratch Register 3 (RTCSCR3) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|---------|--|
| 15-0 | SCRATCH3 | 0-FFFFh | Scratch registers, available to program. |

1.3.26 RTC MSW Scratch Register 4 (RTCSCR4)

The RTC MSW scratch register 4 (RTCSCR4) is shown in [Figure 1-28](#) and described in [Table 1-31](#).

Figure 1-28. RTC MSW Scratch Register 4 (RTCSCR4)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1-31. RTC MSW Scratch Register 4 (RTCSCR4) Field Descriptions

| Bit | Field | Value | Description |
|------|----------|---------|--|
| 15-0 | SCRATCH4 | 0-FFFFh | Scratch registers, available to program. |

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