Pre-lab questions

Q1. Write a C function **initSPI** that initializes the C5515 for communication with slave device 1 with:

- At a frequency of 1 MHz
- SPI communication mode 1
- Interrupts at the end of every frame
- Frames consist of 1 characters

Q2. Write the C functions **readSPI** and **writeSPI** that collect data from and send data to a slave device over SPI, respectively. Please use the following function starter code. Assume you are using SPI1 with character length 16.

```
//readSPI
Uint16 readSPI(){
//your code here
}

//writeSPI
void writeSPI(Uint16 data){
//your code here
}
```

Q3. The following is a segment of Verilog code that is involved in SPI communication. Look over the following code and describe in your own words what is happening. What mode is the DE2-70's master device communicating with?

```
reg [2:0] SSELr;
always @(posedge clk)
      SSELr <= {SSELr[1:0], SSEL};
wire SSEL_active = ~SSELr[1];

always @(posedge clk)
begin
  if(~SSEL_active)
    bitcnt <= 4'b0000;
  else
  begin
           if(SCK_risingedge)
           begin
           bitcnt <= bitcnt + 4'b0001;
           MOSIshift <= {MOSIshift[14:0], MOSI_data};
           end
      end
end
```

Q4. Write a snippet of code that does what the above code does but using SPI mode 3.

Q5. Look back at Figures 7 and 8. You're given that in both diagrams the CLKPOL register is set to 0, and know that CLKPOL tells us when to know a received bit is valid relative to the I2S_CLK signal.

Using those two figures and this knowledge, answer the following question: under CLKPOL = 0, FRMT = 1, what event on the I2S_CLK tells us a bit received is valid? What about under FRMT = 0?

Q6. Let's say you are using I2S and the WDLNGTH is 4 bits and you're not using data packing. Every time you receive an interrupt, you concatenate the data on the receive register to a chunk of a 32 bit number. Explain how you could be more efficient using the I2SCTRL register.

Q7. Write a C function **initializeI2S()** that defines configurations and updates the necessary registers to set up the C5515 as I2S slave in mono mode, DSP format, with active low relative to the frame and expecting to receive on the falling edge of the I2S_CLK.

Q8. Let's say you have a word length of 16 bits and you're in 'stereo' mode. What should your FSDIV be?

In-lab Questions

Q1. You will not immediately see a sine wave from the AIC. The immediate reason is that the AIC is outputting values too small and close to 0. Why might this be? (Think about the input from the Pmod. How many bits does the Pmod send across?) What does this imply about how you need to change the input from the Pmod?

Q2. How many bits do you need to use for bit masking?

Q3. What SPI mode does the Pmod DA2 use?

Q4. You may have noticed the 'steps' in the outputted waveform, the time quantization. How might you reduce this quantization effect?

Q5. How much delay exists between the input and output signals?

Q6. Notice how the **`mosiDataRegister`** is updated in the **`spiSlave`** code, how data shifts to the left. What does this tell us about how we expect the MOSI message to come through?