# Midterm Exam Corrections/Clarifications

**Problem 4:**

- For problem 4 parts D-F, a mapping is for *one* logical-physical register pair, not the entire map table.
- In part F, by resource we mean register

**Problem 6:** SystemVerilog Recursive Generate

- If you run out of space, write in the margins but keep it on the same page
    - Anything not on the page will not be graded

**Problem 7:** SystemVerilog UART Design

- When reset is asserted, the module should return to the idle state.
- Reset is synchronous.
- Hint: The parity bit can be computed using an XOR (the ^ operator in SystemVerilog)

**Problem 8:** R10K Cycles

- The tail points to the youngest instruction in the ROB, NOT the next empty spot
- In cycle 1, r2 maps to p6 and r4 maps to p4+
- In cycle 1, RS entry #1 T2 should be p4+