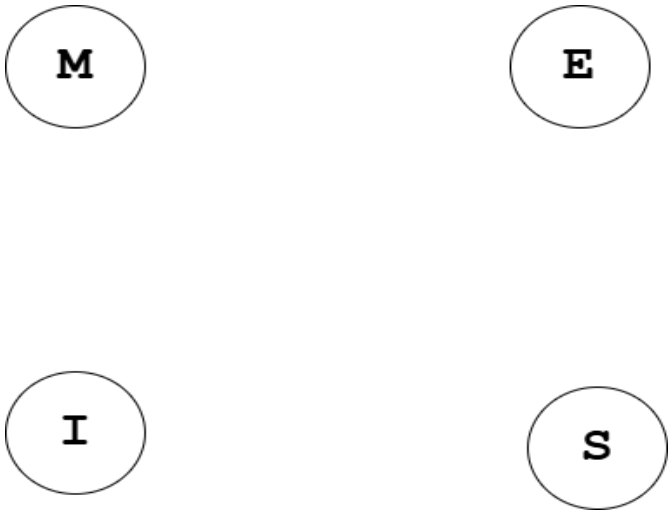
EECS 470 F24 Final Review Session Worksheet

Multiprocessors:

1. Complete the following state diagram for the MESI protocol:



2. Consider 3 processors using a snooping bus-based MESI protocol. All three processors have 2 line direct mapped caches with each line consisting of 16 bytes. The caches begin with all lines marked invalid. Complete the following table (don't worry about HIT/HITM):

Processor	Address	Read/ Write	Bus transaction(s)	Hit/Miss	HIT/ HITM	4C's miss type.
1	0x100	Write				
1	0x200	Read				
2	0x200	Read				
1	0x200	Write				
1	0x110	Write				
1	0x110	Read				
3	0x110	Write				
2	0x100	Read				
3	0x100	Read				
1	0x100	Write				

	Proc 1	
	Address	State
Set 0		
Set 1		

	Proc 2	
	Address	State
Set 0		
Set 1		

	Proc 3	
	Address	State
Set 0		
Set 1		

Virtual Memory and Caches:

1. Consider a 42-bit, byte-addressable system that uses virtual memory. The system has a maximum of 128 GB of physical memory installed with a page size of 8 KB. If we have a hierarchical page table such that each page table level must fit in a single page, how many page table levels would we need to map all of the system's virtual memory? Assume page table entries are still 8B each.

2. A useful formula for determining the maximum allowable cache size that avoids the synonym problem for a VIPT cache given associativity and page size is:

   page size * associativity >= cache size

   Derive the formula above from the more elementary formula that:

   page offset bits >= block offset bits + set index bits

3. Chips'N'Dip Processors are trying to design a set-associative virtually-indexed physically-tagged cache hierarchy. They have designed a TLB with a 3ns access latency, a cache data array with a 6ns latency, a cache tag array with a 4ns latency, tag comparison logic with a 2ns latency, and output multiplexors that can select the steer the appropriate way and block offset to the cache output port in 1ns. What is the best clock frequency they could hope to achieve (assuming the cache access logic is the processor's critical path; neglect any logic that isn't described above.)?