EECS 470 Lab 3 Assignment

Note:

- The lab should be completed individually
- The lab check off is due by **Friday, February 2nd**

1 Introduction

Your assignment for this lab will be to debug two Finite State Machines (FSMs), A and B, for both internal and external errors.

- **Internal errors** are errors within the source files, your SystemVerilog module and testbench files, and can be syntax errors or logical errors.
- **External errors** are errors in how the project is set up, your directory structure, file setup, or build tools like Makefiles.

The lab starts with all the files needed to run and test the two FSMs A and B. The lab folder should contain sub-folders for these: `part_a` and `part_b`, respectively. Note that Part A and Part B are different FSMs that have nothing to do with each other.

In both Part A and Part B there is at least one error. The errors may exist in either the design file or the testbench, but you should not modify the testbench functionality (they have comments describing which sections you can modify).

2 Part A

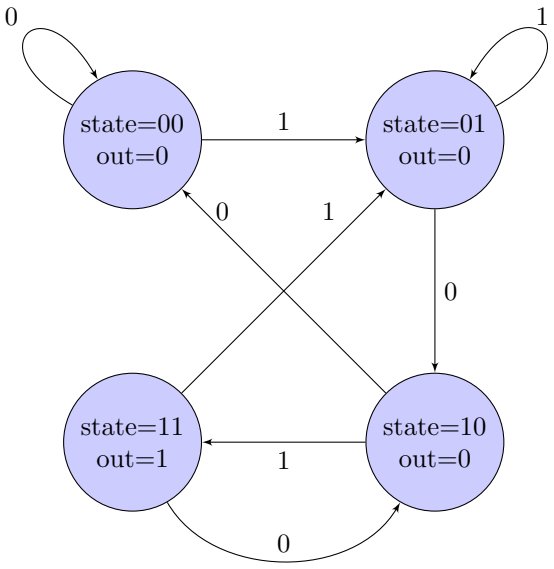

Figure 1: FSM A: The `reset` signal should send the state machine back to state=00. The transition signal for this state machine is labeled `in`.

Fix the errors in this FSM (`fsm_a.sv`) to operate as shown in Fig. 1.

3 Part B

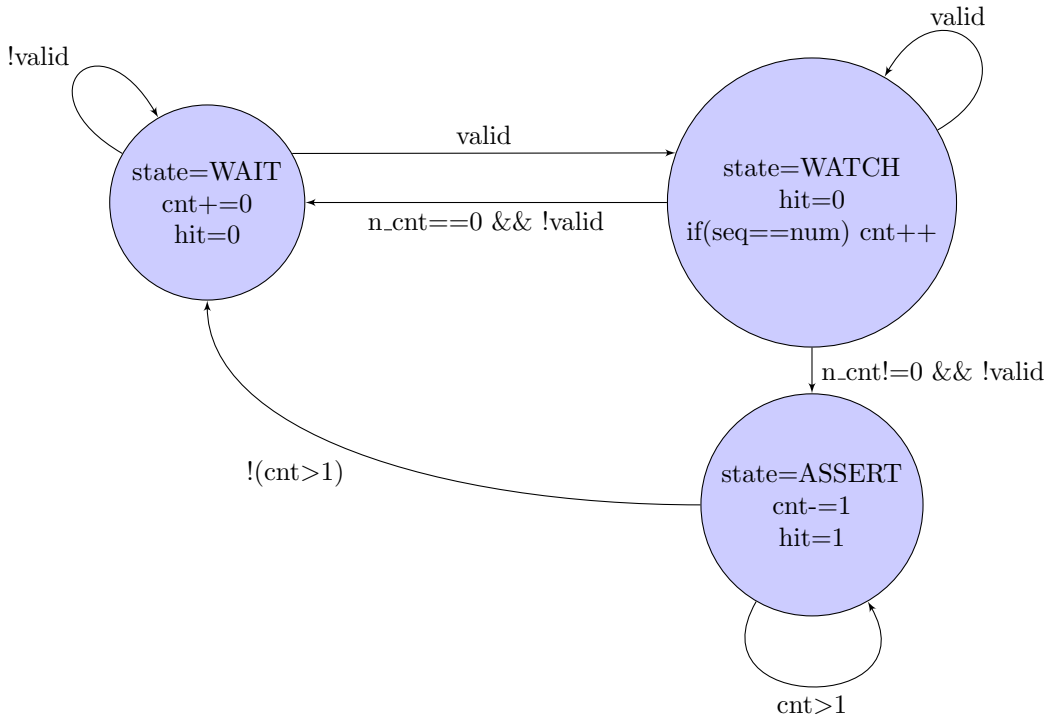

Figure 2: FSM B: The `reset` signal should send the state machine back to state=WAIT and set `cnt` to zero.

Fix the errors in this FSM (`fsm_b.sv`) to operate as shown in Fig. 2.

4 Submission

For lab 3, be ready to show your fixes for the two parts.

Place yourself on the help queue during lab or office hours once you're confident you've completed the lab satisfactorily. Turn in your check-off to Gradescope by the end of the day of next week's lab.