## Helpful Verilog Guidelines

- 1. Spend time designing before you start coding.
- 2. Make your sequential block as simple as possible. They shouldn't have much control flow.
- 3. Use sane and descriptive names for variables. (e.g. tmp is a bad name. What is it a temp of?)
- 4. White space is your friend, but don't abuse it. You want to break code up into related chunks using whitespace.
- 5. Use tabs and spaces in the right places. It is generally best to indent with tabs not spaces. But be consistent.
- 6. Avoid having really long lines of HDL. Wrap code at reasonable places. The code below is a lot more readable formatted this way than it would be if it was all on one line.

- 7. Don't have 7 always\_ff @(posedge clock) blocks when one will do.
- 8. All always\_ff blocks in your behavioral SystemVerilog should register values on the positive edge of the system clock.
- 9. Only change values in a test bench on the negative edge.
- 10. When modeling sequential logic, use nonblocking assignments.
- 11. When modeling combinational logic with an always\_comb block, use blocking assignments.
- 12. Do not mix blocking and nonblocking assignments in the same always block.
- 13. Do not make assignments to the same variable in more than one always block.
- 14. Only use while loops in testbenches.
- 15. For loops don't work like you think, make sure that you understand what they do before using them!
- 16. Don't have initial blocks in Verilog you plan to synthesize.
- 17. Make sure that all paths through an always comb block assign all variables to prevent latches.
- 18. If you follow the above you'll have a much better chance of having synthesizable code that doesn't have race conditions or errors.

Portions Taken from: C. E. Cummings, "Nonblocking Assignments in Verilog Synthesis, Coding Styles That Kill," SNUG 2000. (http://www.sunburst-design.com/papers/CummingsSNUG2000SJ NBA.pdf)