LM3940 1-A Low-Dropout Regulator for 5-V to 3.3-V Conversion

1 Features

- Input Voltage Range: 4.5 V to 5.5 V
- Output Voltage Specified over Temperature
- Excellent Load Regulation
- Specified 1-A Output Current
- Requires only One External Component
- Built-in Protection against Excess Temperature
- Short-Circuit Protected

2 Applications

- Laptop and Desktop Computers
- Logic Systems

3 Description

The LM3940 is a 1-A low-dropout regulator designed to provide 3.3 V from a 5-V supply.

The LM3940 is ideally suited for systems which contain both 5-V and 3.3-V logic, with prime power provided from a 5-V bus.

Because the LM3940 is a true low dropout regulator, it can hold its 3.3-V output in regulation with input voltages as low as 4.5 V.

The TO-220 package of the LM3940 means that in most applications the full 1 A of load current can be delivered without using an additional heatsink.

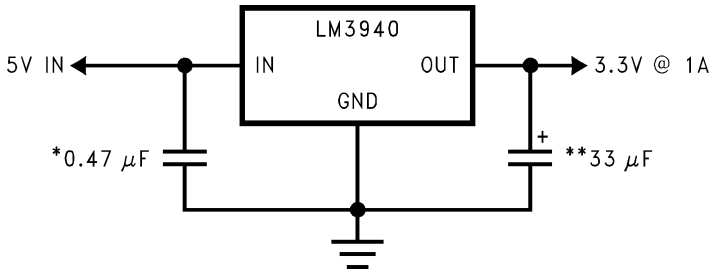
The surface mount DDPAK/TO-263 package uses minimum board space, and gives excellent power dissipation capability when soldered to a copper plane on the PC board.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3940	SOT-223 (4)	6.50 mm x 3.50 mm
	DDPAK/TO-263 (3)	10.18 mm x 8.41 mm
	TO-220 (3)	14.986 mm x 10.16 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



*Required if regulator is located more than 1 inch from the power supply filter capacitor or if battery power is used.
**See *Application and Implementation*.

6.5 Electrical Characteristics

Over operating free-air temperature range, V_{IN} = 5 V, I_{OUT} = 1 A, C_{OUT} = 33 µF (unless otherwise noted). Limits apply for T_J = 25°C, unless otherwise specified in the Test Conditions column.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	5 mA ≤ I_{OUT} ≤ 1 A, T_J = 25°C	3.20	3.3	3.40	V
		5 mA ≤ I_{OUT} ≤ 1 A, –40°C ≤ T_J ≤ 125°C	3.13		3.47	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line regulation	I_{OUT} = 5 mA 4.5 V ≤ V_{IN} ≤ 5.5 V		20	40	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load regulation	50 mA ≤ I_{OUT} ≤ 1 A, T_J = 25°C		35	50	
		50 mA ≤ I_{OUT} ≤ 1 A –40°C ≤ T_J ≤ 125°C		35	80	
Z_{OUT}	Output impedance	I_{OUT} (DC) = 100 mA I_{OUT} (AC) = 20 mA (rms) f = 120 Hz		35		mΩ
I_Q	Quiescent current	4.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 5 mA, T_J = 25°C		10	15	mA
		4.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 5 mA –40°C ≤ T_J ≤ 125°C		10	20	
		V_{IN} = 5 V, I_{OUT} = 1 A, T_J = 25°C		110	200	
		V_{IN} = 5 V, I_{OUT} = 1 A –40°C ≤ T_J ≤ 125°C		110	250	
e_n	Output noise voltage	f_{BW} = 10 Hz – 100 kHz I_{OUT} = 5 mA		150		$\mu V_{(rms)}$
V_{DO}	Dropout voltage(2)	I_{OUT} = 1 A, T_J = 25°C		0.5	0.8	V
		I_{OUT} = 1 A –40°C ≤ T_J ≤ 125°C		0.5	1	
		I_{OUT} = 100 mA, T_J = 25°C		110	150	mV
		I_{OUT} = 100 mA –40°C ≤ T_J ≤ 125°C		110	200	
$I_{OUT(SC)}$	Short-circuit current	R_L = 0	1.2	1.7		A

(1) All limits specified for T_J = 25°C are 100% tested and are used to calculate Outgoing Quality Levels. All limits at temperature extremes are verified via correlation using standard Statistical Quality Control (SQC) methods.
(2) Dropout voltage is defined as the input-output differential voltage where the regulator output drops to a value that is 100 mV below the value that is measured at V_{IN} = 5 V.

OPT3001 Ambient Light Sensor (ALS)

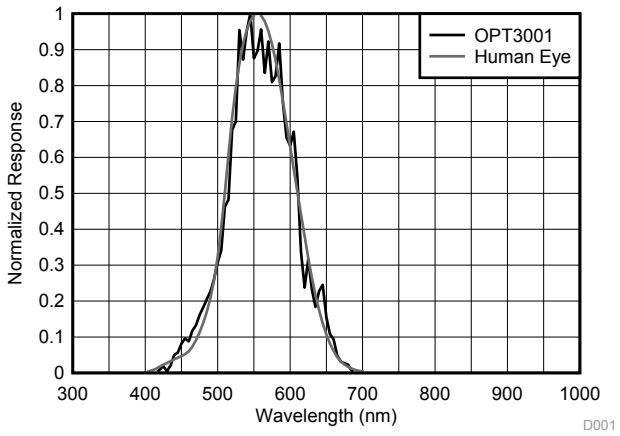
1 Features

- Precision Optical Filtering to Match Human Eye:
  - Rejects > 99% (typ) of IR
- Automatic Full-Scale Setting Feature Simplifies Software and Ensures Proper Configuration
- Measurements: 0.01 lux to 83k lux
- 23-Bit Effective Dynamic Range with Automatic Gain Ranging
- 12 Binary-Weighted Full-Scale Range Settings: < 0.2% (typ) Matching Between Ranges
- Low Operating Current: 1.8 µA (typ)
- Operating Temperature Range: –40°C to +85°C
- Wide Power-Supply Range: 1.6 V to 3.6 V
- 5.5-V Tolerant I/O
- Flexible Interrupt System
- Small-Form Factor: 2.0 mm × 2.0 mm × 0.65 mm

2 Applications

- Display Backlight Controls
- Lighting Control Systems
- Tablet and Notebook Computers
- Thermostats and Home Automation Appliances
- Point-of-Sale Terminals
- Outdoor Traffic and Street Lights
- Cameras

Spectral Response: The OPT3001 and Human Eye



3 Description

The OPT3001 is a sensor that measures the intensity of visible light. The spectral response of the sensor tightly matches the photopic response of the human eye and includes significant infrared rejection.

The OPT3001 is a single-chip lux meter, measuring the intensity of light as visible by the human eye. The precision spectral response and strong IR rejection of the device enables the OPT3001 to accurately meter the intensity of light as seen by the human eye regardless of light source. The strong IR rejection also aids in maintaining high accuracy when industrial design calls for mounting the sensor under dark glass for aesthetics. The OPT3001 is designed for systems that create light-based experiences for humans, and an ideal preferred replacement for photodiodes, photoresistors, or other ambient light sensors with less human eye matching and IR rejection.

Measurements can be made from 0.01 lux up to 83k lux without manually selecting full-scale ranges by using the built-in, full-scale setting feature. This capability allows light measurement over a 23-bit effective dynamic range.

The digital operation is flexible for system integration. Measurements can be either continuous or single-shot. The control and interrupt system features autonomous operation, allowing the processor to sleep while the sensor searches for appropriate wake-up events to report via the interrupt pin. The digital output is reported over an I^2C- and SMBus-compatible, two-wire serial interface.

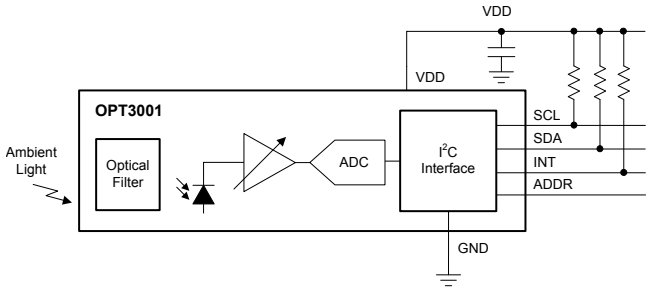
The low power consumption and low power-supply voltage capability of the OPT3001 enhance the battery life of battery-powered systems.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPT3001	USON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Block Diagram



5 Pin Configuration and Functions

DNP Package
USON-6
(Top View)

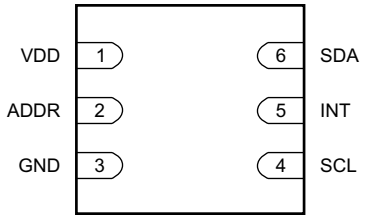


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VDD	Power	Device power. Connect to a 1.6-V to 3.6-V supply.
2	ADDR	Digital input	Address pin. This pin sets the LSBs of the I^2C address.
3	GND	Power	Ground
4	SCL	Digital input	I^2C clock. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
5	INT	Digital output	Interrupt output open-drain. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
6	SDA	Digital input/output	I^2C data. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.

6.5 Electrical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CT = 1)(1), automatic full-scale range (RN[3:0] = 1100b(1)), white LED, and normal-angle incidence of light, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPTICAL							
	Peak irradiance spectral responsivity				550		nm
	Resolution (LSB)	Lowest full-scale range, RN[3:0] = 0000b(1)			0.01		lux
	Full-scale illuminance				83865.6		lux
	Measurement output result	0.64 lux per ADC code, 2620.80 lux full-scale (RN[3:0] = 0110)(1), 2000 lux input(2)		2812	3125	3437	ADC codes
				1800	2000	2200	lux
	Relative accuracy between gain ranges(3)				0.2%		
	Infrared response (850 nm)(2)				0.2%		
	Light source variation (incandescent, halogen, fluorescent)	Bare device, no cover glass			4%		
	Linearity	Input illuminance > 40 lux			2%		
		Input illuminance < 40 lux			5%		
	Measurement drift across temperature	Input illuminance = 2000 lux			0.01		%/°C
	Dark condition, ADC output	0.01 lux per ADC code			0	3	ADC codes
					0	0.03	lux
	Half-power angle	50% of full-power reading			47		degrees
PSRR	Power-supply rejection ratio	V_{DD} at 3.6 V and 1.6 V			0.1		%/V(4)
POWER SUPPLY							
V_{DD}	Operating range			1.6		3.6	V
V_{I^2C}	Operating range of I^2C pull-up resistor	I^2C pull-up resistor, $V_{DD} \le V_{I^2C}$		1.6		5.5	V
I_Q	Quiescent current	Dark	Active, V_{DD} = 3.6 V		1.8	2.5	µA
			Shutdown (M[1:0] = 00)(1), V_{DD} = 3.6 V		0.3	0.47	µA
		Full-scale lux	Active, V_{DD} = 3.6 V		3.7		µA
			Shutdown, (M[1:0] = 00)(1)		0.4		µA
POR	Power-on-reset threshold	T_A = 25°C			0.8		V
DIGITAL							
	I/O pin capacitance				3		pF
	Total integration time(5)	(CT = 1)(1), 800-ms mode, fixed lux range		720	800	880	ms
		(CT = 0)(1), 100-ms mode, fixed lux range		90	100	110	ms
V_{IL}	Low-level input voltage (SDA, SCL, and ADDR)			0		0.3 × V_{DD}	V
V_{IH}	High-level input voltage (SDA, SCL, and ADDR)			0.7 × V_{DD}		5.5	V
I_{IL}	Low-level input current (SDA, SCL, and ADDR)				0.01	0.25(6)	µA
V_{OL}	Low-level output voltage (SDA and INT)	I_{OL}= 3 mA				0.32	V
I_{ZH}	Output logic high, high-Z leakage current (SDA, INT)	Pin at V_{DD}			0.01	0.25(6)	µA
TEMPERATURE							
	Specified temperature range			–40		85	°C

(1) Refers to a control field within the configuration register.
(2) Tested with the white LED calibrated to 2k lux and an 850-nm LED.
(3) Characterized by measuring fixed near-full-scale light levels on the higher adjacent full-scale range setting.
(4) PSRR is the percent change of the measured lux output from its current value, divided by the change in power supply voltage, as characterized by results from 3.6-V and 1.6-V power supplies.
(5) The conversion time, from start of conversion until the data are ready to be read, is the integration time plus 3 ms.
(6) The specified leakage current is dominated by the production test equipment limitations. Typical values are much smaller.

6.6 Timing Requirements(1)

		MIN	TYP	MAX	UNIT
I²C FAST MODE					
f_{SCL}	SCL operating frequency	0.01		0.4	MHz
t_{BUF}	Bus free time between stop and start	1300			ns
t_{HDSTA}	Hold time after repeated start	600			ns
t_{SUSTA}	Setup time for repeated start	600			ns
t_{SUSTO}	Setup time for stop	600			ns
t_{HDDAT}	Data hold time	20		900	ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_{RC} and t_{FC}	Clock rise and fall time			300	ns
t_{RD} and t_{FD}	Data rise and fall time			300	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms
I²C HIGH-SPEED MODE					
f_{SCL}	SCL operating frequency	0.01		2.6	MHz
t_{BUF}	Bus free time between stop and start	160			ns
t_{HDSTA}	Hold time after repeated start	160			ns
t_{SUSTA}	Setup time for repeated start	160			ns
t_{SUSTO}	Setup time for stop	160			ns
t_{HDDAT}	Data hold time	20		140	ns
t_{SUDAT}	Data setup time	20			ns
t_{LOW}	SCL clock low period	240			ns
t_{HIGH}	SCL clock high period	60			ns
t_{RC} and t_{FC}	Clock rise and fall time			40	ns
t_{RD} and t_{FD}	Data rise and fall time			80	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms

(1) All timing parameters are referenced to low and high voltage thresholds of 30% and 70%, respectively, of final settled value.

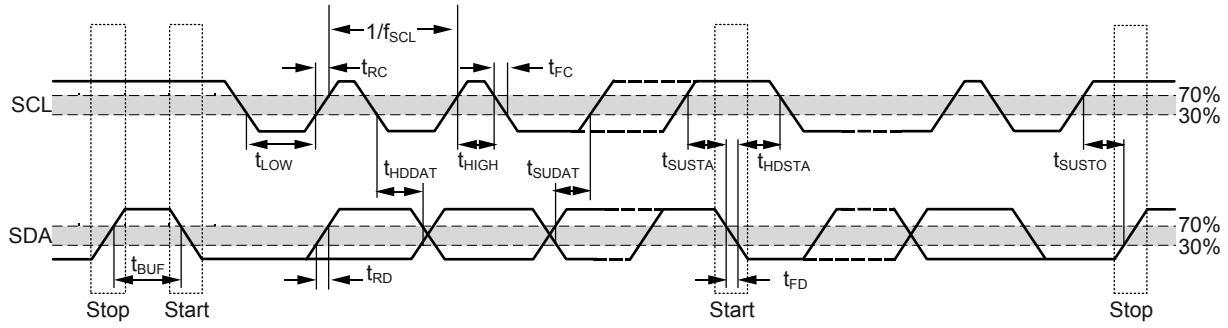


Figure 1. I²C Detailed Timing Diagram

7 Detailed Description

7.1 Overview

The OPT3001 measures the ambient light that illuminates the device. This device measures light with a spectral response very closely matched to the human eye, and with very good infrared rejection.

Matching the sensor spectral response to that of the human eye response is vital because ambient light sensors are used to measure and help create ideal human lighting experiences. Strong rejection of infrared light, which a human does not see, is a crucial component of this matching. This matching makes the OPT3001 especially good for operation underneath windows that are visibly dark, but infrared transmissive.

The OPT3001 is fully self-contained to measure the ambient light and report the result in lux digitally over the I^2C bus. The result can also be used to alert a system and interrupt a processor with the INT pin. The result can also be summarized with a programmable window comparison and communicated with the INT pin.

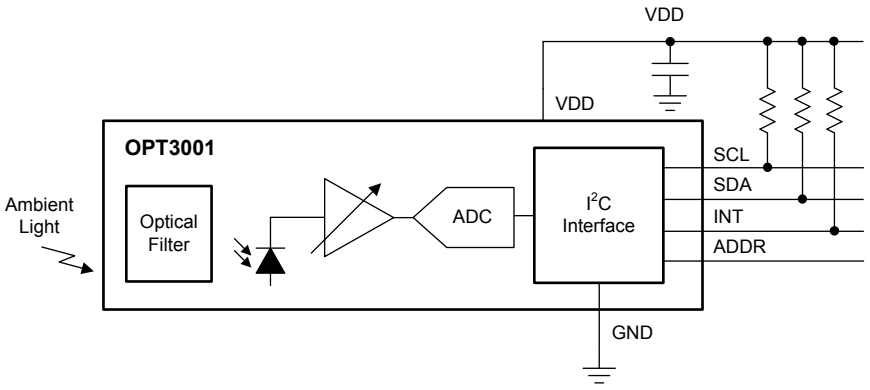
The OPT3001 can be configured into an automatic full-scale, range-setting mode that always selects the optimal full-scale range setting for the lighting conditions. This mode frees the user from having to program their software for potential iterative cycles of measurement and readjustment of the full-scale range until optimal for any given measurement. The device can be commanded to operate continuously or in single-shot measurement modes.

The device integrates its result over either 100 ms or 800 ms, so the effects of 50-Hz and 60-Hz noise sources from typical light bulbs are nominally reduced to a minimum.

The device starts up in a low-power shutdown state, such that the OPT3001 only consumes active-operation power after being programmed into an active state.

The OPT3001 optical filtering system is not excessively sensitive to non-ideal particles and micro-shadows on the optical surface. This reduced sensitivity is a result of the relatively minor device dependency on uniform-density optical illumination of the sensor area for infrared rejection. Proper optical surface cleanliness is always recommended for best results on all optical devices.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Human Eye Matching

The OPT3001 spectral response closely matches that of the human eye. If the ambient light sensor measurement is used to help create a good human experience, or create optical conditions that are optimal for a human, the sensor must measure the same spectrum of light that a human sees.

The device also has excellent infrared light (IR) rejection. This IR rejection is especially important because many real-world lighting sources have significant infrared content that humans do not see. If the sensor measures infrared light that the human eye does not see, then a true human experience is not accurately represented.

Furthermore, if the ambient light sensor is hidden underneath a dark window (such that the end-product user cannot see the sensor) the infrared rejection of the OPT3001 becomes significantly more important because many dark windows attenuate visible light but transmit infrared light. This attenuation of visible light and lack of attenuation of IR light amplifies the ratio of the infrared light to visible light that illuminates the sensor. Results can still be well matched to the human eye under this condition because of the high infrared rejection of the OPT3001.

7.3.2 Automatic Full-Scale Range Setting

The OPT3001 has an automatic full-scale range setting feature that eliminates the need to predict and set the optimal range for the device. In this mode, the OPT3001 automatically selects the optimal full-scale range for the given lighting condition. The OPT3001 has a high degree of result matching between the full-scale range settings. This matching eliminates the problem of varying results or the need for range-specific, user-calibrated gain factors when different full-scale ranges are chosen. For further details, see the *Automatic Full-Scale Setting Mode* section.

7.3.3 Interrupt Operation, INT Pin, and Interrupt Reporting Mechanisms

The device has an interrupt reporting system that allows the processor connected to the I^2C bus to go to sleep, or otherwise ignore the device results, until a user-defined event occurs that requires possible action. Alternatively, this same mechanism can also be used with any system that can take advantage of a single digital signal that indicates whether the light is above or below levels of interest.

The interrupt event conditions are controlled by the high-limit and low-limit registers, as well as the configuration register latch and fault count fields. The results of comparing the result register with the high-limit register and low-limit register are referred to as *fault events*. The fault count register dictates how many consecutive same-result fault events are required to trigger an interrupt event and subsequently change the state of the interrupt reporting mechanisms, which are the INT pin, the flag high field, and the flag low field. The latch field allows a choice between a latched window-style comparison and a transparent hysteresis-style comparison.

The INT pin has an open-drain output, which requires the use of a pull-up resistor. This open-drain output allows multiple devices with open-drain INT pins to be connected to the same line, thus creating a logical *NOR* or *AND* function between the devices. The polarity of the INT pin can be controlled with the polarity of interrupt field in the configuration register. When the POL field is set to 0, the pin operates in an active low behavior that pulls the pin low when the INT pin becomes active. When the POL field is set to 1, the pin operates in an active high behavior and becomes high impedance, thus allowing the pin to go high when the INT pin becomes active.

Additional details of the interrupt reporting registers are described in the *Interrupt Reporting Mechanism Modes* and *Internal Registers* sections.

Feature Description (continued)

7.3.4 I²C Bus Overview

The OPT3001 offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another. The I²C interface is used throughout this document as the primary example with the SMBus protocol specified only when a difference between the two protocols is discussed.

The OPT3001 is connected to the bus with two pins: an SCL clock input pin and an SDA open-drain bidirectional data pin. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates start and stop conditions. To address a specific device, the master initiates a start condition by pulling the data signal line (SDA) from a high logic level to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge bit by pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition. When all data are transferred, the master generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The OPT3001 includes a 28-ms timeout on the I²C interface to prevent locking up the bus. If the SCL line is held low for this duration of time, the bus state machine is reset.

7.3.4.1 Serial Bus Address

To communicate with the OPT3001, the master must first initiate an I²C start command. Then, the master must address slave devices via a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

Four I²C addresses are possible by connecting the ADDR pin to one of four pins: GND, VDD, SDA, or SCL. Table 2 summarizes the possible addresses with the corresponding ADDR pin configuration. The state of the ADDR pin is sampled on every bus communication and must be driven or connected to the desired level before any activity on the interface occurs.

Table 2. Possible I²C Addresses with Corresponding ADDR Configuration

DEVICE I²C ADDRESS	ADDR PIN
1000100	GND
1000101	VDD
1000110	SDA
1000111	SCL

7.3.4.2 Serial Interface

The OPT3001 operates as a slave device on both the I²C bus and SMBus. Connections to the bus are made via the SCL clock input line and the SDA open-drain I/O line. The OPT3001 supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). All data bytes are transmitted most-significant bits first.

The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. See the *Electrical Interface* section for further details of the I²C bus noise immunity.

7.4 Device Functional Modes

7.4.1 Automatic Full-Scale Setting Mode

The OPT3001 has an automatic full-scale-range setting mode that eliminates the need for a user to predict and set the optimal range for the device. This mode is entered when the configuration register range number field (RN[3:0]) is set to 1100b.

The first measurement that the device takes in auto-range mode is a 10-ms range assessment measurement. The device then determines the appropriate full-scale range to take its first full measurement.

For subsequent measurements, the full-scale range is set by the result of the previous measurement. If a measurement is towards the low side of full-scale, the full-scale range is decreased by one or two settings for the next measurement. If a measurement is towards the upper side of full-scale, the full-scale range is increased by one setting for the next measurement.

If the measurement exceeds the full-scale range, resulting from a fast increasing optical transient event, the current measurement is aborted. This invalid measurement is not reported. A 10-ms measurement is taken to assess and properly reset the full-scale range. Then, a new measurement is taken with this proper full-scale range. Therefore, during a fast increasing optical transient in this mode, a measurement can possibly take longer to complete and report than indicated by the configuration register conversion time field (CT).

7.4.2 Interrupt Reporting Mechanism Modes

There are two major types of interrupt reporting mechanism modes: latched window-style comparison mode and transparent hysteresis-style comparison mode. The configuration register latch field (L) (see the configuration register, bit 4) controls which of these two modes is used. An end-of-conversion mode is also associated with each major mode type. The end-of-conversion mode is active when the two most significant bits of the threshold low register are set to 11b. The mechanisms report via the flag high and flag low fields, the conversion ready field, and the INT pin.

7.4.2.1 Latched Window-Style Comparison Mode

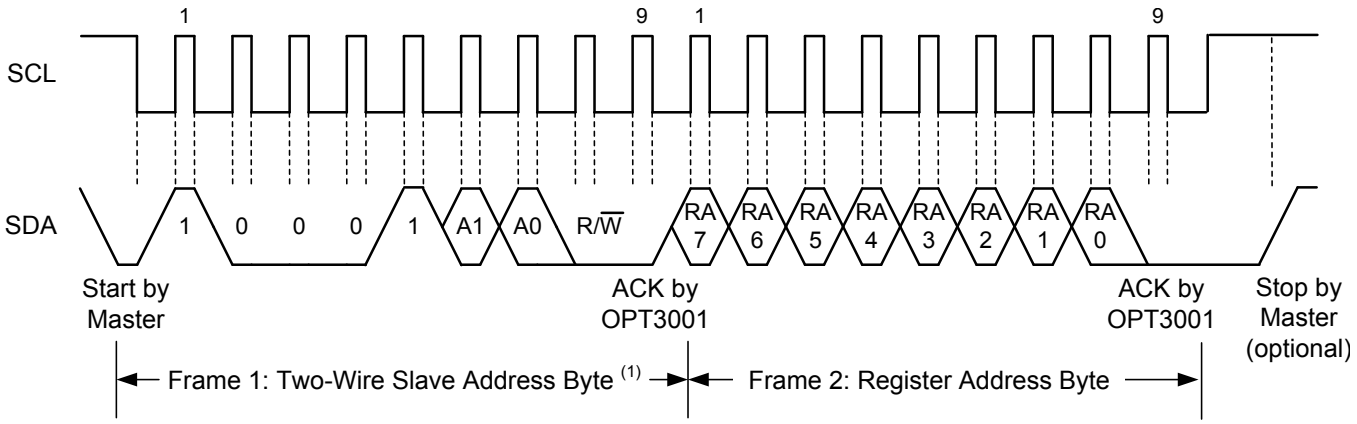
The latched window-style comparison mode is typically selected when using the OPT3001 to interrupt an external processor. In this mode, a fault is recognized when the input signal is above the high-limit register or below the low-limit register. When the consecutive fault events trigger the interrupt reporting mechanisms, these mechanisms are latched, thus reporting whether the fault is the result of a high or low comparison. These mechanisms remain latched until the configuration register is read, which clears the INT pin and flag high and flag low fields. The SMBus alert response protocol, described in detail in the *SMBus Alert Response* section, clears the pin but does not clear the flag high and flag low fields. The behavior of this mode, along with the conversion ready flag, is summarized in Table 3. Note that Table 3 does not apply when the two threshold low register MSBs (see the *Transparent Hysteresis-Style Comparison Mode* section for clarification on the MSBs) are set to 11b.

7.5 Programming

The OPT3001 supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). Fast and standard modes are described as the default protocol, referred to as *F/S*. High-speed mode is described in the *High-Speed I²C Mode* section.

7.5.1 Writing and Reading

Accessing a specific register on the OPT3001 is accomplished by writing the appropriate register address during the I²C transaction sequence. Refer to Table 7 for a complete list of registers and their corresponding register addresses. The value for the register address (as shown in Figure 19) is the first byte transferred after the slave address byte with the R/W bit low.



(1) The value of the slave address byte is determined by the ADDR pin setting; see Table 2.

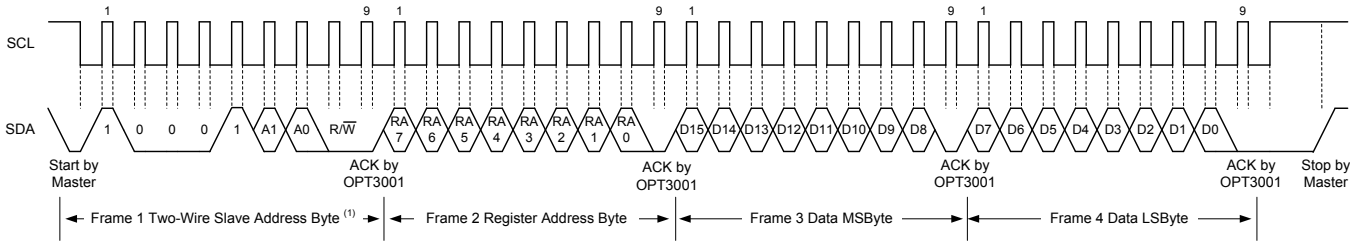
Figure 19. Setting the I²C Register Address

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address with the R/W bit low. The OPT3001 then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register that data are to be written to. The next two bytes are written to the register addressed by the register address. The OPT3001 acknowledges receipt of each data byte. The master may terminate the data transfer by generating a start or stop condition.

When reading from the OPT3001, the last value stored in the register address by a write operation determines which register is read during a read operation. To change the register address for a read operation, a new partial I²C write transaction must be initiated. This partial write is accomplished by issuing a slave address byte with the R/W bit low, followed by the register address byte and a stop command. The master then generates a start condition and sends the slave address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register address. This byte is followed by an acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate the data transfer by generating a not-acknowledge after receiving any data byte, or by generating a start or stop condition. If repeated reads from the same register are desired, continually sending the register address bytes is not necessary; the OPT3001 retains the register address until that number is changed by the next write operation.

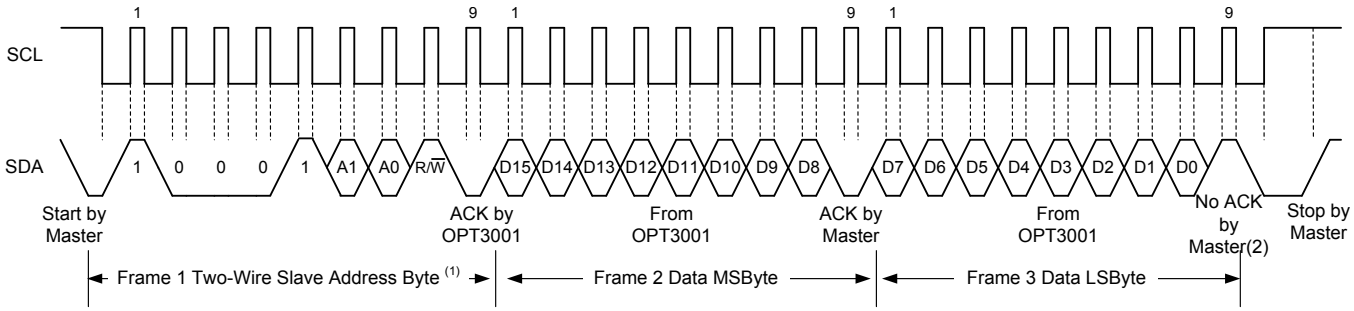
Programming (continued)

Figure 20 and Figure 21 show the write and read operation timing diagrams, respectively. Note that register bytes are sent most significant byte first, followed by the least significant byte.



(1) The value of the slave address byte is determined by the setting of the ADDR pin; see Table 2.

Figure 20. I²C Write Example



(1) The value of the slave address byte is determined by the ADDR pin setting; see Table 2.

(2) An ACK by the master can also be sent.

Figure 21. I²C Read Example

7.5.1.1 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up resistors or active pull-up devices. The master generates a start condition followed by a valid serial byte containing the high-speed (HS) master code 0000 1XXXb. This transmission is made in either standard mode or fast mode (up to 400 kHz). The OPT3001 does not acknowledge the HS master code but does recognize the code and switches its internal filters to support a 2.6-MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.6 MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS mode. A stop condition ends the HS mode and switches all internal filters of the OPT3001 to support the F/S mode.

7.5.1.2 General-Call Reset Command

The I²C general-call reset allows the host controller in one command to reset all devices on the bus that respond to the general-call reset command. The general call is initiated by writing to the I²C address 0 (0000 0000b). The reset command is initiated when the subsequent second address byte is 06h (0000 0110b). With this transaction, the device issues an acknowledge bit and sets all of its registers to the power-on-reset default condition.

7.6 Register Maps

7.6.1 Internal Registers

The device is operated over the I^2C bus with registers that contain configuration, status, and result information. All registers are 16 bits long.

There are four main registers: result, configuration, low-limit, and high-limit. There are also two ID registers: manufacturer ID and device ID. Table 7 lists these registers.

Table 7. Register Map

REGISTER	ADDRESS (Hex)(1)	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Result	00h	E3	E2	E1	E0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
Configuration	01h	RN3	RN2	RN1	RN0	CT	M1	M0	OVF	CRF	FH	FL	L	POL	ME	FC1	FC0
Low Limit	02h	LE3	LE2	LE1	LE0	TL11	TL10	TL9	TL8	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
High Limit	03h	HE3	HE2	HE1	HE0	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
Manufacturer ID	7Eh	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Device ID	7Fh	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0

(1) Register offset and register address are used interchangeably.

7.6.1.1 Register Descriptions

NOTE
Register offset and register address are used interchangeably.

7.6.1.1.1 Result Register (offset = 00h)

This register contains the result of the most recent light to digital conversion. This 16-bit register has two fields: a 4-bit exponent and a 12-bit mantissa.

Figure 23. Result Register (Read-Only)

15	14	13	12	11	10	9	8
E3	E2	E1	E0	R11	R10	R9	R8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	R1	R0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 8. Result Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	E[3:0]	R	0h	**Exponent.** These bits are the exponent bits. Table 9 provides further details.
11:0	R[11:0]	R	000h	**Fractional result.** These bits are the result in straight binary coding (zero to full-scale).

Table 9. Full-Scale Range and LSB Size as a Function of Exponent Level

E3	E2	E1	E0	FULL-SCALE RANGE (lux)	LSB SIZE (lux per LSB)
0	0	0	0	40.95	0.01
0	0	0	1	81.90	0.02
0	0	1	0	163.80	0.04
0	0	1	1	327.60	0.08
0	1	0	0	655.20	0.16
0	1	0	1	1310.40	0.32
0	1	1	0	2620.80	0.64
0	1	1	1	5241.60	1.28
1	0	0	0	10483.20	2.56
1	0	0	1	20966.40	5.12
1	0	1	0	41932.80	10.24
1	0	1	1	83865.60	20.48

The formula to translate this register into lux is given in Equation 1:

$$lux = LSB\_Size \times R[11:0] \quad (1)$$

where:

$$LSB\_Size = 0.01 \times 2^{E[3:0]} \quad (2)$$

LSB_Size can also be taken from Table 9. The complete lux equation is shown in Equation 3:

$$lux = 0.01 \times (2^{E[3:0]}) \times R[11:0] \quad (3)$$

A series of result register output examples with the corresponding LSB weight and resulting lux are given in Table 10. Note that many combinations of exponents (E[3:0]) and fractional results (R[11:0]) can map onto the same lux result, as shown in the examples of Table 10.

Table 10. Examples of Decoding the Result Register into lux

RESULT REGISTER (Bits 15:0, Binary)	EXPONENT (E[3:0], Hex)	FRACTIONAL RESULT (R[11:0], Hex)	LSB WEIGHT (lux, Decimal)	RESULTING LUX (Decimal)
0000 0000 0000 0001b	00h	001h	0.01	0.01
0000 1111 1111 1111b	00h	FFFh	0.01	40.95
0011 0100 0101 0110b	03h	456h	0.08	88.80
0111 1000 1001 1010b	07h	89Ah	1.28	2818.56
1000 1000 0000 0000b	08h	800h	2.56	5242.88
1001 0100 0000 0000b	09h	400h	5.12	5242.88
1010 0010 0000 0000b	0Ah	200h	10.24	5242.88
1011 0001 0000 0000b	0Bh	100h	20.48	5242.88
1011 0000 0000 0001b	0Bh	001h	20.48	20.48
1011 1111 1111 1111b	0Bh	FFFh	20.48	83865.60

Note that the exponent field can be disabled (set to zero) by enabling the exponent mask (configuration register, ME field = 1) and manually programming the full-scale range (configuration register, RN[3:0] < 1100b (0Ch)), allowing for simpler operation in a manually-programmed, full-scale mode. Calculating lux from the result register contents only requires multiplying the result register by the LSB weight (in lux) associated with the specific programmed full-scale range (see Table 9). See the Low-Limit Register for details.

See the configuration register conversion time field (CT, bit 11) description for more information on lux resolution as a function of conversion time.

7.6.1.1.2 Configuration Register (offset = 01h) [reset = C810h]

This register controls the major operational modes of the device. This register has 11 fields, which are documented below. If a measurement conversion is in progress when the configuration register is written, the active measurement conversion immediately aborts. If the new configuration register directs a new conversion, that conversion is subsequently started.

Figure 24. Configuration Register

15	14	13	12	11	10	9	8
RN3	RN2	RN1	RN0	CT	M1	M0	OVF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
7	6	5	4	3	2	1	0
CRF	FH	FL	L	POL	ME	FC1	FC0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only

Table 11. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RN[3:0]	R/W	1100b	**Range number field (read or write).** The range number field selects the full-scale lux range of the device. The format of this field is the same as the result register exponent field (E[3:0]); see Table 9. When RN[3:0] is set to 1100b (0Ch), the device operates in automatic full-scale setting mode, as described in the *Automatic Full-Scale Setting Mode* section. In this mode, the automatically chosen range is reported in the result exponent (register 00h, E[3:0]). The device powers up as 1100 in automatic full-scale setting mode. Codes 1101b, 1110b, and 1111b (0Dh, 0Eh, and 0Fh) are reserved for future use.

Table 11. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CT	R/W	1b	**Conversion time field (read or write).** The conversion time field determines the length of the light to digital conversion process. The choices are 100 ms and 800 ms. A longer integration time allows for a lower noise measurement. The conversion time also relates to the effective resolution of the data conversion process. The 800-ms conversion time allows for the fully specified lux resolution. The 100-ms conversion time with full-scale ranges above 0101b for E[3:0] in the result and configuration registers also allows for the fully specified lux resolution. The 100-ms conversion time with full-scale ranges below and including 0101b for E[3:0] can reduce the effective result resolution by up to three bits, as a function of the selected full-scale range. Range 0101b reduces by one bit. Ranges 0100b, 0011b, 0010b, and 0001b reduces by two bits. Range 0000b reduces by three bits. The result register format and associated LSB weight does not change as a function of the conversion time. 0 = 100 ms 1 = 800 ms
10:9	M[1:0]	R/W	00b	**Mode of conversion operation field (read or write).** The mode of conversion operation field controls whether the device is operating in continuous conversion, single-shot, or low-power shutdown mode. The default is 00b (shutdown mode), such that upon power-up, the device only consumes operational level power after appropriately programming the device. When single-shot mode is selected by writing 01b to this field, the field continues to read 01b while the device is actively converting. When the single-shot conversion is complete, the mode of conversion operation field is automatically set to 00b and the device is shut down. When the device enters shutdown mode, either by completing a single-shot conversion or by a manual write to the configuration register, there is no change to the state of the reporting flags (conversion ready, flag high, flag low) or the INT pin. These signals are retained for subsequent read operations while the device is in shutdown mode. 00 = Shutdown (default) 01 = Single-shot 10, 11 = Continuous conversions
8	OVF	R	0b	**Overflow flag field (read-only).** The overflow flag field indicates when an overflow condition occurs in the data conversion process, typically because the light illuminating the device exceeds the programmed full-scale range of the device. Under this condition OVF is set to 1, otherwise OVF remains at 0. The field is reevaluated on every measurement. If the full-scale range is manually set (RN[3:0] field < 1100b), the overflow flag field can be set while the result register reports a value less than full-scale. This result occurs if the input light has a temporary high spike level that temporarily overloads the integrating ADC converter circuitry but returns to a level within range before the conversion is complete. Thus, the overflow flag reports a possible error in the conversion process. This behavior is common to integrating-style converters. If the full-scale range is automatically set (RN[3:0] field = 1100b), the only condition that sets the overflow flag field is if the input light is beyond the full-scale level of the entire device. When there is an overflow condition and the full-scale range is not at maximum, the OPT3001 aborts its current conversion, sets the full-scale range to a higher level, and starts a new conversion. The flag is set at the end of the process. This process repeats until there is either no overflow condition or until the full-scale range is set to its maximum range.
7	CRF	R	0b	**Conversion ready field (read-only).** The conversion ready field indicates when a conversion completes. The field is set to 1 at the end of a conversion and is cleared (set to 0) when the configuration register is subsequently read or written with any value except one containing the shutdown mode (mode of operation field, M[1:0] = 00b). Writing a shutdown mode does not affect the state of this field; see the *Interrupt Reporting Mechanism Modes* section for more details.
6	FH	R	0b	**Flag high field (read-only).** The flag high field (FH) identifies that the result of a conversion is larger than a specified level of interest. FH is set to 1 when the result is larger than the level in the high-limit register (register address 03h) for a consecutive number of measurements defined by the fault count field (FC[1:0]). See the *Interrupt Reporting Mechanism Modes* section for more details on clearing and other behaviors of this field.
5	FL	R	0b	**Flag low field (read-only).** The flag low field (FL) identifies that the result of a conversion is smaller than a specified level of interest. FL is set to 1 when the result is smaller than the level in the low-limit register (register address 02h) for a consecutive number of measurements defined by the fault count field (FC[1:0]). See the *Interrupt Reporting Mechanism Modes* section for more details on clearing and other behaviors of this field.

Table 11. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	L	R/W	1b	**Latch field (read or write).** The latch field controls the functionality of the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL). This bit selects the reporting style between a latched window-style comparison and a transparent hysteresis-style comparison. 0 = The device functions in transparent hysteresis-style comparison operation, where the three interrupt reporting mechanisms directly reflect the comparison of the result register with the high- and low-limit registers with no user-controlled clearing event. See the *Interrupt Operation, INT Pin, and Interrupt Reporting Mechanisms* section for further details. 1 = The device functions in latched window-style comparison operation, latching the interrupt reporting mechanisms until a user-controlled clearing event.
3	POL	R/W	0b	**Polarity field (read or write).** The polarity field controls the polarity or active state of the INT pin. 0 = The INT pin reports active low, pulling the pin low upon an interrupt event. 1 = Operation of the INT pin is inverted, where the INT pin reports active high, becoming high impedance and allowing the INT pin to be pulled high upon an interrupt event.
2	ME	R/W	0b	**Mask exponent field (read or write).** The mask exponent field forces the result register exponent field (register 00h, bits E[3:0]) to 0000b when the full-scale range is manually set, which can simplify the processing of the result register when the full-scale range is manually programmed. This behavior occurs when the mask exponent field is set to 1 and the range number field (RN[3:0]) is set to less than 1100b. Note that the masking is only performed to the result register. When using the interrupt reporting mechanisms, the result comparison with the low-limit and high-limit registers is unaffected by the ME field.
1:0	FC[1:0]	R/W	00b	**Fault count field (read or write).** The fault count field instructs the device as to how many consecutive fault events are required to trigger the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL). The fault events are described in the latch field (L), flag high field (FH), and flag low field (FL) descriptions. 00 = One fault count (default) 01 = Two fault counts 10 = Four fault counts 11 = Eight fault counts

Application Information (continued)

The visible-spectrum transmission for dark windows typically ranges between 5% to 30%, but can be less than 1%. Specify a visible-spectrum transmission as low as, but no more than, necessary to achieve sufficient visual appeal because decreased transmission decreases the available light for the sensor to measure. The windows are made dark by either applying an ink to a transparent window material, or including a dye or other optical substance within the window material itself. This attenuating transmission in the visible spectrum of the window creates a ratio between the light on the outside of the design and the light that is measured by the OPT3001. To accurately measure the light outside of the design, compensate the OPT3001 measurement for this ratio; an example is given in Dark Window Selection and Compensation.

Ambient light sensors are used to help create ideal lighting experiences for humans; therefore, the matching of the sensor spectral response to that of the human eye response is vital. Infrared light is not visible to the human eye, and can interfere with the measurement of visible light when sensors lack infrared rejection. Therefore, the ratio of visible light to interfering infrared light affects the accuracy of any practical system that represents the human eye. The strong rejection of infrared light by the OPT3001 allows measurements consistent with human perception under high-infrared lighting conditions, such as from incandescent, halogen, or sunlight sources.

Although the inks and dyes of dark windows serve their primary purpose of being minimally transmissive to visible light, some inks and dyes can also be very transmissive to infrared light. The use of these inks and dyes further decreases the ratio of visible to infrared light, and thus decreases sensor measurement accuracy. However, because of the excellent infrared rejection of the OPT3001, this effect is minimized, and good results are achieved under a dark window with similar spectral responses to those shown in Figure 31.

For best accuracy, avoid grill-like window structures, unless the designer understands the optical effects sufficiently. These grill-like window structures create a nonuniform illumination pattern at the sensor that make light measurement results vary with placement tolerances and angle of incidence of the light. If a grill-like structure is desired, the OPT3001 is an excellent sensor choice because it is minimally sensitive to illumination uniformity issues disrupting the measurement process.

Light pipes can appear attractive for aiding in the optomechanical design that brings light to the sensor; however, do not use light pipes with any ambient light sensor unless the system designer fully understands the ramifications of the optical physics of light pipes within the full context of his design and objectives.

8.2 Typical Application

Measuring the ambient light with the OPT3001 in a product case and under a dark window is described in this section. The schematic for this design is shown in Figure 29.

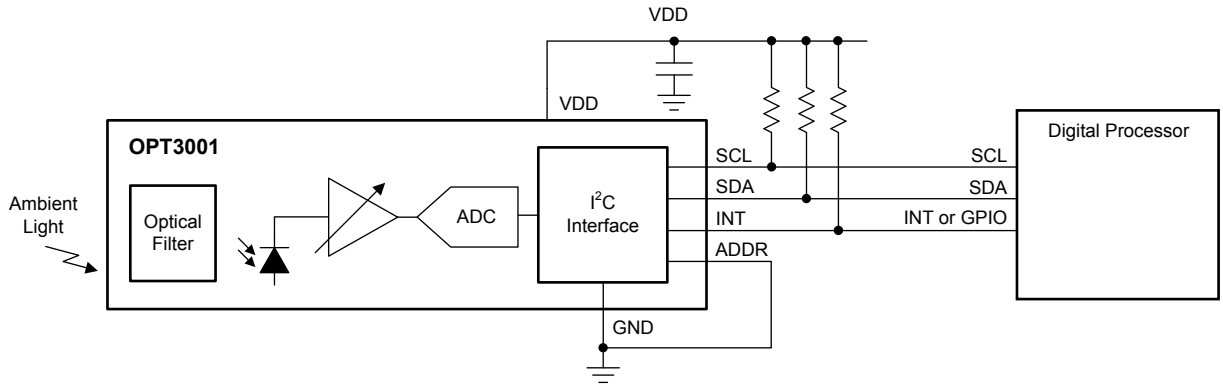


Figure 29. Measuring Ambient Light in a Product Case Behind a Dark Window

9 Power-Supply Recommendations

Although the OPT3001 has low sensitivity to power-supply issues, good practices are always recommended. For best performance, the OPT3001 V_{DD} pin must have a stable, low-noise power supply with a 100-nF bypass capacitor close to the device and solid grounding. There are many options for powering the OPT3001 because the device current consumption levels are very low.

List of Arduino APIs:

I2C

#include <Wire.h>

Wire.beginTransmission(addr); // Begin a transmission to the I2C slave device with the given address.
// Subsequently, queue bytes for transmission with the write() function
// and transmit them by calling endTransmission().

Wire.write(val); // Writes data from a slave device in response to a request from a
// master, or queues bytes for transmission from a master to slave
// device (in-between calls to beginTransmission() and
// endTransmission()).

Wire.endTransmission(); // Ends a transmission to a slave device that was begun by
// beginTransmission() and transmits the bytes that were queued by
// write().

Wire.requestFrom(addr, num) //Send read request for 'num' bytes to device with I2C address 'addr'

Wire.available() //Is data we've asked to read available on the I2C bus? Returns
//how many bytes are available.

Wire.read() // Reads a byte that was transmitted from a slave device to a master
// after a call to requestFrom() or was transmitted from a master to a
// slave

Note: *Only the pin A4 and A5 can be used as I2C pins. It is set automatically by the Wire library. A4 is SDA and A5 is SCL.*

I2C example

```
#include <Wire.h>
void setup()
{
  Wire.begin();        // join i2c bus (address optional for master)
  Serial.begin(9600);  // start serial for output
}

void loop()
{
  Wire.requestFrom(2, 6);    // request 6 bytes from slave device #2
  while(Wire.available())    // slave may send less than requested
  {
    char c = Wire.read();    // receive a byte as character
    Serial.print(c);         // print the character
  }

  delay(500);
}
```

Digital I/O

pinMode(pin, mode) //mode is INPUT, OUTPUT or INPUT_PULLUP

digitalWrite(pin, value) //Write value HIGH/LOW at GPIO 'pin'

digitalRead(pin) // Reads the value from a specified digital pin, either HIGH or LOW.

LCD

The default LCD library is used to print the results on the LCD

LCD.begin(cols, rows) //Set number of columns and rows

LCD.setcursor(col, row) //Set cursor at col and row

LCD.print(data) //data: It can be char, int, string

LCD.write(char) // write one character

Misc

delay(val); // Delays the program for 'val' milliseconds

pow(x,y); // returns the value x^y (x and y are floats, the return value is a double).
// So pow(3,2) returns 9.0.