Passive RFID Tag with UWB Transmitter

Seunghyun Lee, Seunghyun Oh, and Yonghyun Shim

***Abstract*—Radio Frequency Identification Tag is a transmitter which transmits its own identification to interrogators and has been used in many areas such as tracking and distribution industries. The main issues of passive RFID tag are power harvesting and low power consumption. Previous works usually involved antenna backscattering method and special fabrication technique to minimize power consumption [1],[2]. However, a UWB transmitter can provide better immunity to multipath problem with less power consumption [3]. In this project, essential blocks for a passive RF-ID Tag with UWB Transmitter with reading distance of 10m will be implemented without using any specialized fabrication technique.**

***Index Terms*— RFID, UWB, Power harvesting, Injection Locking**

I. Introduction

RFID tags are widely used in a variety of tracking, security and tagging applications. Compared to a conventional barcode system, it does not require a light of sight reading condition, and it can provide unique information for each product. However, as cost of a single RFID tag is much expensive than a simple bar code, these tags have to be manufactured with standard process to be economically viable. There are two different types of RFID tag: passive and active systems. Active RF-ID tag utilizes battery to supply power to the system. On the other hand, a passive system usually extracts its power from wireless signal. A passive system cannot achieve farther reading distance compared to an active one, but it can be used permanently and implemented with less cost. As for transmission, it is possible to use a transmitter or backscattering method. Using additional transmitter usually consumes more power, but it gives several benefits [1], [2]. For example, a UWB transmitter is more resistant to multi path interference and has lower energy consumption.

In this paper, we propose a passive RFID tag with UWB transmitter which can achieve 10m reading distance. The center frequency of power harvesting is 915 MHZ which gives less attenuation compared to 2.45 GHZ. This design will only require standard 0.13 um CMOS technology and no additional fabrication technology such as Schottky diode [1], or Silicon on Sapphire [2]. System Overview

A. Architecture

The entire system of this application is described in Fig. 1. Voltage Multiplier, Clock Generator, and UWB transmitter are implemented and tested in this project whereas antenna, matching network, ROM, and other digital control circuits are not included. This RF-ID tag is designed to deliver 128 bit information at 10 m distance from interrogator.

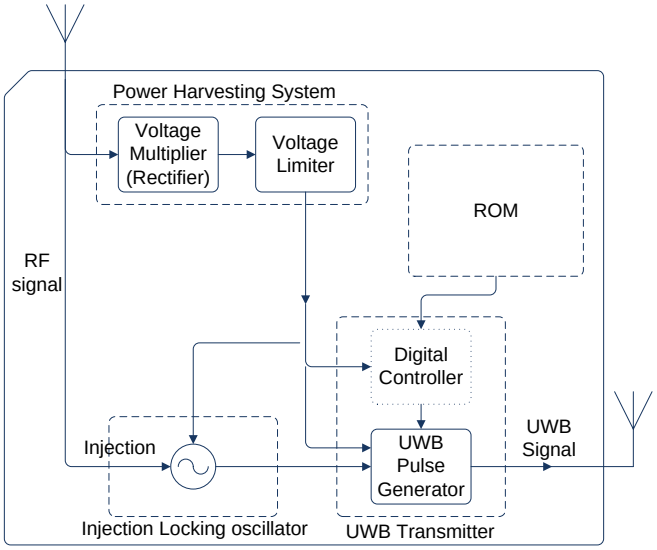

Fig. 1. Overall Architecture

B. System Environment

The receiving power from antenna is attenuated as distance between interrogator and RF-ID tag increases. The relationship between distance and receiving power is equal to

$$P_r = P_{EIRP} G_r \left(\frac{\lambda_{RF}}{4\pi d}\right)^2 \quad (1)$$

where P_{EIRP} is power of RF signal from a interrogator, λ_{RF} is a wavelength of RF signal, G_r is a antenna gain of RF-ID Tag, and d is distance between interrogator and RF-ID tag. It is also important to select the proper center frequency of input RF signal. Equation (1) suggests that RF signal with higher center frequency is attenuated more. For the proposed device, a 915 MHz RF input signal will be used for wireless power harvesting. This frequency belongs to ISM band, and its maximum output power from source is restricted by FCC to 1 W, 4W EIRP. With target distance of 10 m, this power will be attenuated to 27.23 UW. The main challenge here is to supply sufficient DC voltage for the entire system and the minimize power consumption.

II. Power Harvesting

A. Interface between Antenna and Rectifier

The input RF signal from interrogator should be changed to DC bias, in order to supply voltage to the entire system. Fig. 2 shows a single stage of full-wave rectifier. As the input voltage amplitude of antenna with 50 Ohms radiation resistance is only about 50 mV, the rectifier in Fig. 2 will not work. The input voltage of antenna is

$$V_{load} = 2\sqrt{2R_S P_{EIRP}\left(\frac{\lambda_{RF}}{4\pi d}\right)^2 \frac{R_L}{R_L + R_S}} \qquad (2)$$

where R_S is the radiation resistance of antenna, and R_L is the resistance of the voltage multiplier [2].

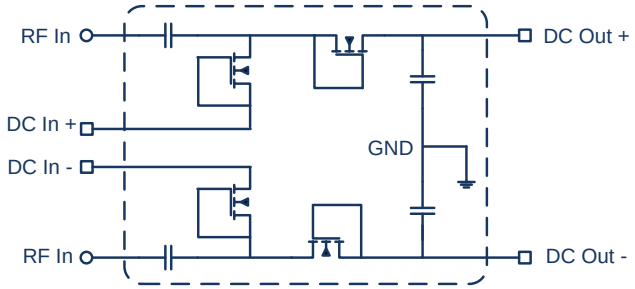

Fig. 2. Single Stage of Full-Wave Rectifier

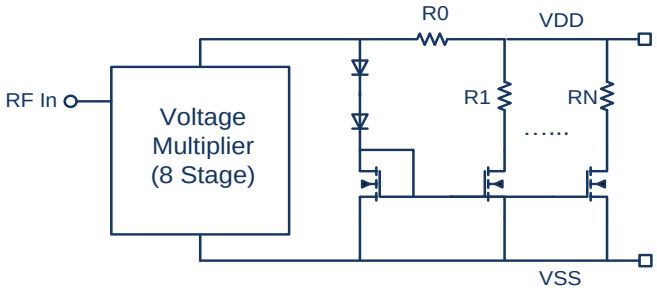

Fig. 3. 8 Stage Voltage Multiplier and Limiter

This equation shows that higher radiation resistance gives higher input amplitude of voltage. However, radiation resistance more than 500 Ohms is not usually used because the Q factor in matching network is low and there is more power loss. In this project, antenna with radiation resistance of 300 Ohms is assumed, which was already proved to show good performance [2]. In this case, the amplitude of input voltage is 127.82 mV, but it is still low to drive general diode connected mosfets. To overcome this low input voltage, zero threshold voltage nfet in IBM 0.13 μm is used.

We did not add a matching network between antenna and the voltage multiplier because the input impedance of the voltage multiplier was difficult to expect. Furthermore, as the MIM capacitance, which has minimum parasitic loss, is at least 60 fF in our process, there is some limitation in choosing matching network elements. However, if proper matching network is implementable, the use of matching network could improve the available load power.

A. *Voltage Multiplier and Limiter*

Eight stages of Full-wave Rectifier and a voltage Limiter are shown in Fig. 3. The minimum requirement of the bias voltage in our system should be more than 1.2 V. Therefore, to achieve a maximum reading distance of 10 m, the input voltage amplitude, 127.82 mV should be boosted up to at least 10 times. In the ideal case, as each full-wave rectifier can make 4 times of input peak amplitude, it only requires 3 stages of full-wave rectifier. However, voltage drop and reverse leakage in the zero threshold fet reduce the voltage gain. As

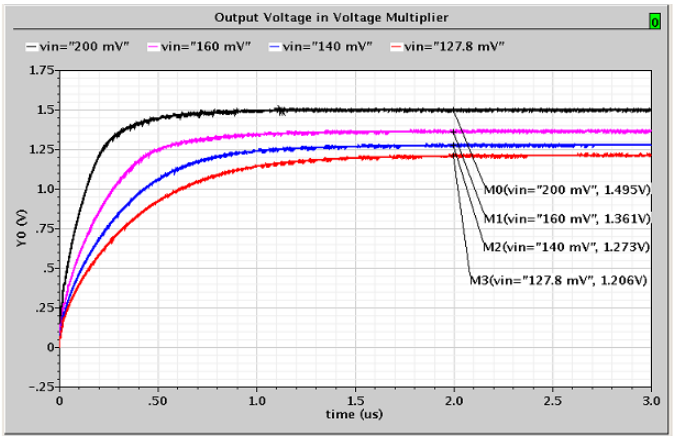

Fig. 4. 8 Stage Voltage Multiplier and Limiter

the voltage drop of zero thresholds FET is about 80 mV in average, each stage only gives 200 mV gain. Thus, to achieve 1.4 V output voltage, the total number of stage should be more than eight.

One of the issue in this voltage boosting rectifier is that the output voltage can increase too much as the distance is close to the interrogator. Therefore, the output voltage limiter should be used to protect other components from being damaged. The circuit on the right side of Fig. 3 is a simple limiter which can limit output voltage less than 3 V. For better limiter performance, it would be better to use more mirror stages. However, since the increased mirrored stage gives more loss in the minimum power distance of 10 m, the number of stage is limited to two as the output voltage still becomes more than 1.2 V.

B. *Simulation Result*

The several output voltages of voltage multiplier and limiter are shown in Fig. 4. From the output voltage amplitude and output current, the output power can be calculated as 1.12 μW, which is approximately 4.12% of incident power, 27.34 μW. This is relatively smaller efficiency than usual case. This is because more number of stages should be used to achieve the minimum required output voltage. Due to the limiter, the output voltage does not increase linearly. The simulation result of higher input voltage is not attached due to the simulation convergence problem. For more stable operation, the increase of limiter stages will be required.

III. Injection Locking and Clock Extraction

In this system, the clock is extracted from the incident RF signal using an injection locking oscillator. This method is far more power efficient than a PLL or a Schmitt trigger method [4], [5].

A. *Locking Mechanism and Design Methodology*

Injection locked oscillator can be modeled as a nonlinear block, followed by a RLC tank in a positive feedback loop as shown in Fig. 5. If output frequency is denoted as $\omega_o = \omega_t + \Delta\omega$ where ω_t is the tank resonance frequency and $\Delta\omega$ is the offset frequency, it can be shown that [5],

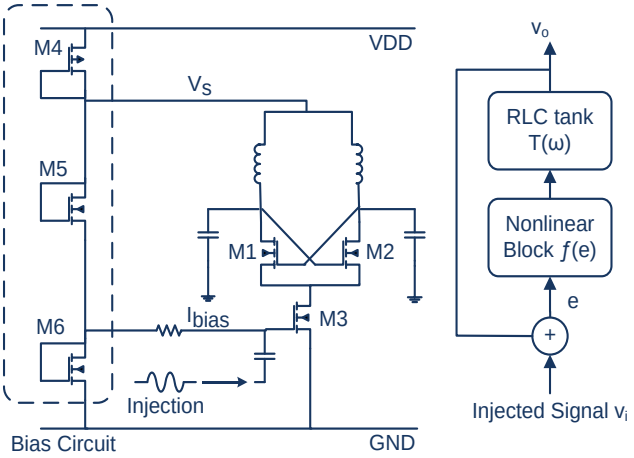

Fig. 5. Schematic and Block Model of Injection Locked Oscillator

$$\left|\frac{\Delta\omega}{\omega_t}\right| < \left|c\frac{\omega L V_i}{2}\right| \quad (3)$$

As (1) suggests, the locking range can be increased by either increasing incident signal amplitude V_i or the inductance L of the RLC tank. Hence Inductance L was maximized and M1 and M2 were sized so that g_m was large enough for oscillation. I_{bias} and V_s was chosen to operate in current limited region for least power dissipation [6]. V_{DD} was fixed to 1.2 V but the supply voltage V_s was lowered to 850mV to reduce power consumption.

B. *Performance*

Transient response of the oscillator locked to an incident signal of 915MHz is shown in Fig. 7. The fast Fourier transform shows its first harmonics at 915.5MHz. Oscillator lock in delay was 20ns and the amplitude was 800mV_{peak}. Center frequency of free-running oscillator was found to be 916.6MHz. The locking range for different incident RF signal strength is plotted in Fig. 6. At 10m distance (around 128mV), lock-in range of 896MHz to 933MHz was achieved. Lock-in frequency error was less than 0.3% of its actual value.

Monte Carlo simulation (Fig.8) shows that of center frequency of the free running oscillator will change significantly over the process corners. However, the lock-in range was not affected by process or temperature corners. This means that LC tank will vary in center frequency but the lock-in range will be large enough so that it will lock-in to the desired 915MHz signal. Fig 8. shows that 96% of the device will be operate at 10m range(130mV signal strength).

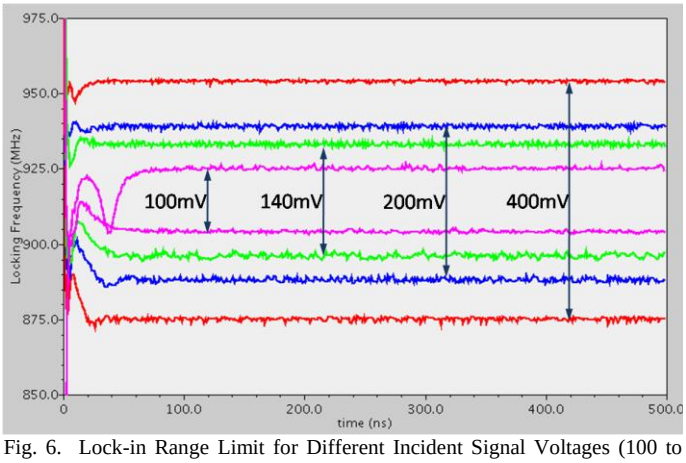

Fig. 6. Lock-in Range Limit for Different Incident Signal Voltages (100 to 400mV)

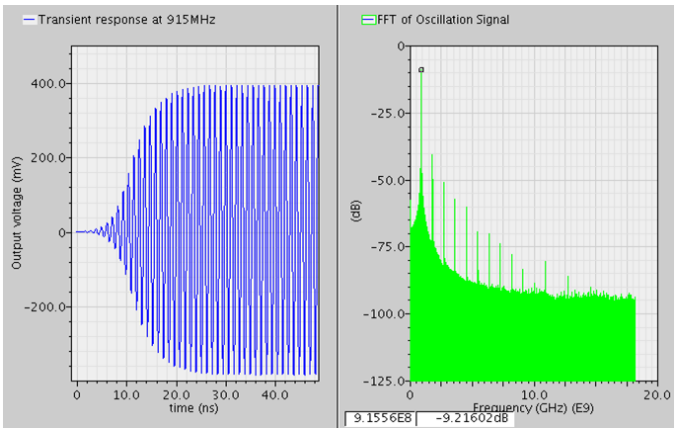

Fig. 7. Transient Response of Injection locked State and FFT of Oscillation Signal

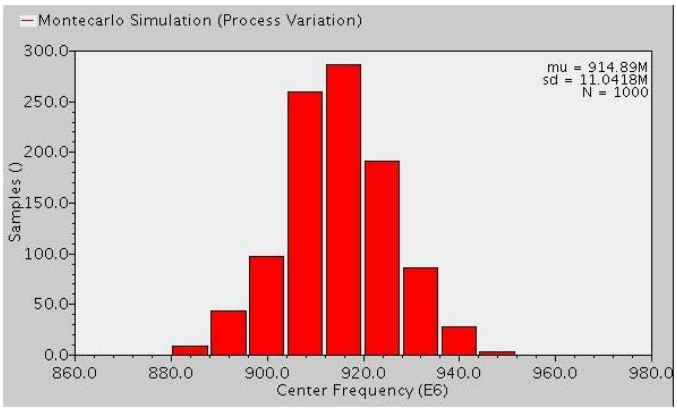

Fig. 8 Device working range over process variation with 140mV incident signal

Phase noise (Fig.9) was found to be -86dBc at an offset of 100KHz for free running oscillator. Oscillator frequency over supply variation of 0.9 to 1.3V was also investigated. The oscillator was still able to lock-in with 0.4 V of V_{dd} variations.

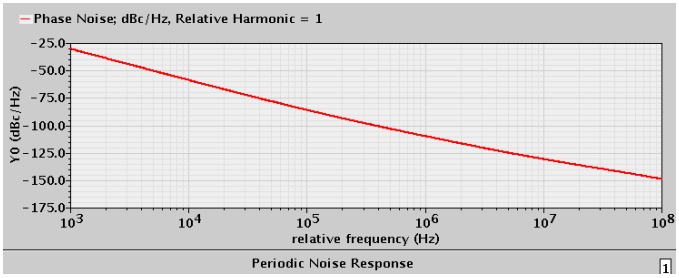

Fig. 9 Phase Noise Plot and Frequency Pulling from Supply Variation

IV. UWB Pulse Generator

A. *Differential to Single ended block.*

The proposed clock must have full VDD swing and be single-ended. Since the output of LC oscillator has small differential output (400mV), we need a circuit which makes differential inputs to single-ended output and also amplifies the signal. The topology of circuit is shown as Fig. 10. It is a two stage op-amp with single ended output. The power consumption is 160uW.

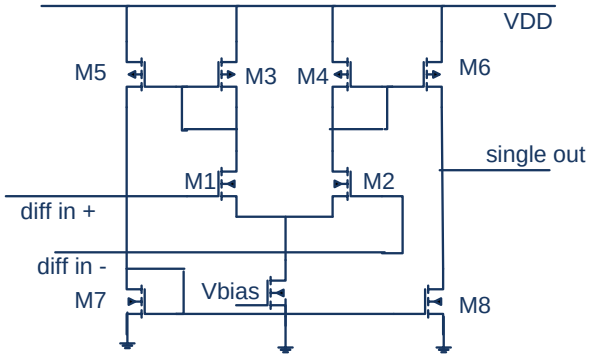

Fig. 10. Two Stage OP Amp with Single Ended Output

B. *UWB Pulse Generator*

For UWB transmitter, we will use a 4.5GHz pulse whose frequency is 5 times the clock signal (915MHz). From the LC oscillator, we can get square wave 915 MHz clock. Square wave which have same duty cycle can be express as :

$$f(x) = \frac{4}{\pi} \sum_{i=1,3,5,7\ldots} \frac{1}{n} \sin\left(\frac{n\pi x}{T}\right) \qquad (4)$$

where T is the period. This expression means that it has only odd order harmonics and no other frequency component. Therefore it is good to use bandpass filter to extract fifth harmonic of clock. However, the amplitude of fifth order harmonic signal is too small, we need to use amplifier. In this case, we used CMOS inverter with feedback. The DC point of CMOS inverter output is the threshold of inverter. Therefore we can use inverter to get a full swing pulse.
Inverter amplifier spends 350uW and inverters before LC bandpass filter and after inverter amplifier use 100uW.

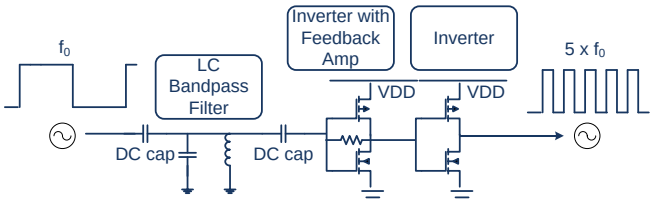

Fig. 11. Clock Multiplication

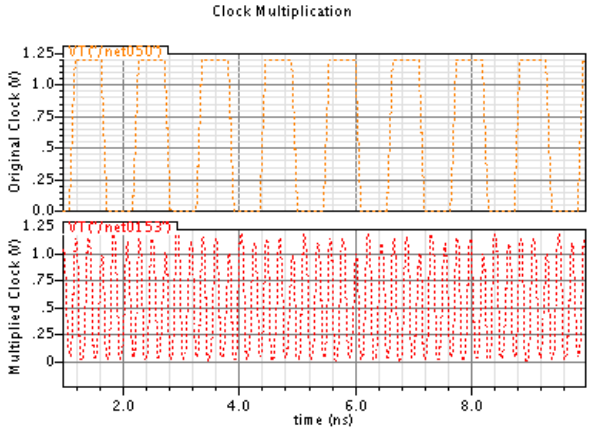

Fig. 12. Simulation Result of Clock Multiplication

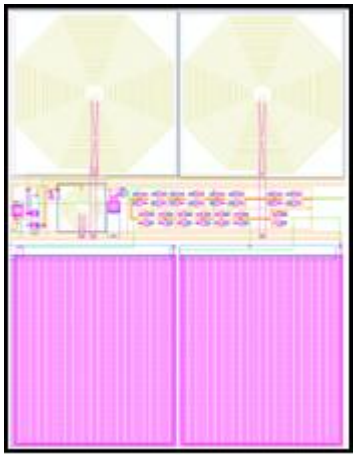

Fig. 13. Overall Layout

In the maximum reading distance, the variation should be less than 0.1 V. The total expected power consumption is 610 μW, and time duration is 256 ns for transmission of 128 bits. Therefore, output capacitances should be at least 1.6 nF, which are quite large, two 400 μm by 480 μm dual MIM caps should be used. With a initial condition, the charging time of this cap is about 1ms. Fig. 13. is the layout of our RF-ID Tag, 850 μm by 1050 μm.

V. Conclusion

In this project, we suggest passive RF-ID Tag which can achieve 10 m reading distance. To achieve this distance, larger charge tank is used, so overall area is increased. Further work is implementing ROM and control logic. Additional regulating system could be also used for more stable performance, but there would be additional power loss. This low power, passive RF-ID tag system can be also used with various sensors with a shorter reading distance.

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