A Low Phase Noise and Low Power Frequency Synthesizer for GSM Up-conversion

Mao-Ter Chen, BoQiang Xiao, Chung Chiang Wu

***Abstract*— Phase Lock Loops are used extensively in communications. This paper discusses a frequency synthesizer for generating the LO signal for up-conversion in GSM cell phones. This synthesizer takes a low frequency input clock and uses a phase lock loop / fractional N divider circuit to generate an output LO signal for the up-conversion mixer. It will be able lock onto any of the 124 channels within the 890-915MHz bandwidth used for GSM up-conversion. This synthesizer is designed for low phase noise and low power, the two most critical parameters for mobile cell phone applications.**

***Index Terms*— Phase Lock Loop, GSM, Dual Modulus, Phase Frequency Detector, Charge Pump, Voltage Controlled Oscillator.**

I. Introduction

THE top level design for a basic frequency synthesizer is composed of a phase detector, LPF, voltage controlled oscillator, and feedback divider for frequency multiplication. To improve the lock acquisition of the synthesizer, we designed a phase frequency detector. A charge pump was added at the output of the PFD to source / sink current and manage the voltage on the LPF. This voltage (V_{CONT}), is used to control the capacitance of the LC tank of the VCO and set the oscillation frequency of the synthesizer output. Finally, a dual modulus divider (DMD) with an imbedded prescaler was used to dither between dividing by 32/33 to set the output frequency as a fractional multiple of the input reference frequency. With an input reference frequency of 27.8MHz, the output frequency is

$$f_{out} = \left(N + \frac{dither}{count}\right) * f_{ref}$$
$$where\ N = 32,\ \ count = 139,\ \ \&\ \ dither \in [1,139]$$

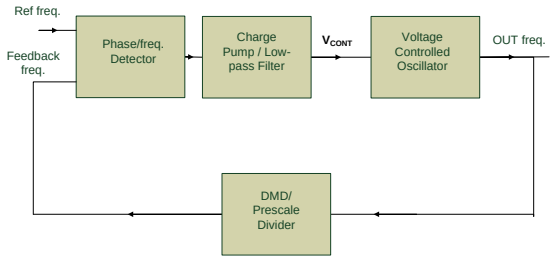

Figure 1: System Level Block Diagram

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Mao-Ter Chen is a Master's Student at the University of Michigan, Ann Arbor, MI 48109 USA (e-mail: stefanyc@umich.edu).

BoQiang Xiao is a Master's Student at the University of Michigan, Ann Arbor, MI 48109 USA (e-mail: xiaobo@umich.edu).

Chung Chiang Wu is a PHD Student at the University of Michigan, Ann Arbor, MI 48109 USA (e-mail: chungwu@umich.edu).

II. Block Level Design

A. Phase Frequency Detector and Charge Pump / LPF

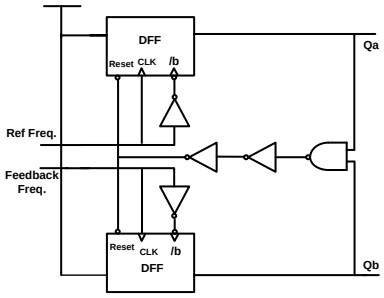

Figure 2: CMOS PFD Block Diagram, Flip-Flop Latch Design

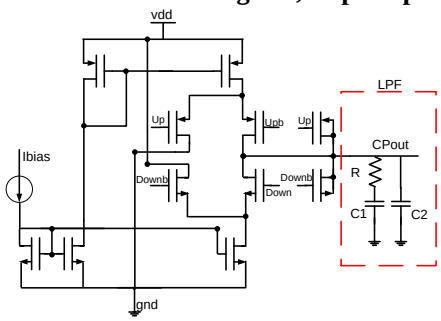

Figure 3: Charge Pump and LPF

The PFD implementation is a circuit whose average output V_{OUT} is linearly proportional to its input phase difference $\Delta\varphi$. Due to finite V_{CONT} rise and falltimes resulting from large capacitances seen at low pass filter charging node, short PFD output pulses will have problems turning on the CP to charge/discharge the LPF adequately (deadzone). A stable V_{CONT} is critical for low phase noise and low lock time. Therefore, in order to minimize deadzone while providing a stable control voltage for VCO, improvements were made to the design. First, the PFD was designed with a delayed reset to be able to capture smaller input phase differences, which minimizes dead zone. Our deadzone is less than 10ps with a reference frequency of 27.8MHz. This is less than 0.017rad, with near minimum sized reset delay buffers to conserve PFD power.

When the phase difference is detected, a charge pump consisting of two switched current sources charges or discharges the loop filter in accordance with the PDF output pulses. A power conservative reference current of 50µA is used with current mirrors for this design and was adequate for a stable V_{CONT}. However, the current switching introduces voltage spikes on V_{CONT}, so a MOS capacitive divider was used to abate these spikes.

To design for a lock settling time of 4µ:

$$T_S = \frac{16\pi}{\omega_n} \quad \rightarrow \quad \omega_n = 2\pi * 16\ \frac{Krad}{s} \qquad \text{(eq.1)}$$

where ω_n is the natural frequency of the closed loop phase transfer function for the synthesizer. We also chose a damping factor ζ to be slightly higher than 0.707 to be overdamped, which achieves the best settling time. Hence, the closed loop bandwidth is approximated as:

$$\omega_B = \omega_n \sqrt{2\zeta^2+1+\sqrt{(2\zeta^2+1)^2+1}} = 2\pi * 33 \quad \frac{Krad}{s} \qquad \text{(eq.2)}$$

We chose to add the series RC portion of the LPF in order to add a zero to the system for greater stability. However, it also introduces a pole. Making C_2 small relative to C_1 ($C_2 \approx 0.1C_1$) will push that pole frequency much higher than the zero, increasing stability. To design the LPF resistor and capacitor values:

$$C_1 = \frac{I_p K_{VCO}}{2\pi \times N\omega_n^2} \approx 2.0nF\ ,\ C_2 = 0.1C_1, \&\ R = \frac{2\zeta}{\omega_n C_1} = 5.9k\Omega$$

(eq.3, refer to fig.3 for label mapping)

Due to the large size of these capacitors, we decided to leave the LPF off-chip.

B. Voltage Controlled Oscillator

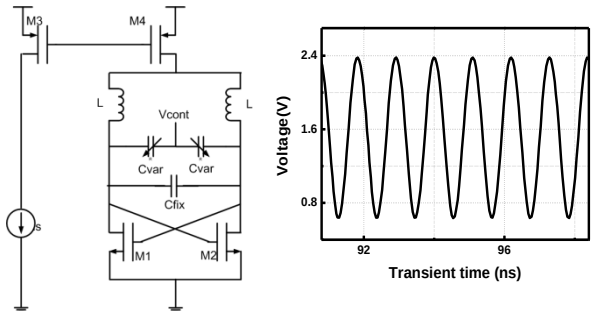

Figure 4: a) VCO Schematic b) VCO output at 890 MHz

The schematic view of the implemented VCO is shown as Fig. 4. The cross-coupled NMOS differential pairs provide negative transconductance ($-g_m$) to compensate the parasitic losses in the parallel RLC tank at resonance. A PMOS current mirror is used to supply to bias current, since PMOS transistors have lower flicker noise than NMOS transistors. Next, we used on-chip spiral inductors. Designing an inductor for maximum LC tank Q is important in VCO design because:

$Q \uparrow = R_P \uparrow = I_{bias} \downarrow$ for the same V_{swing} (Justification below). This lowers our power consumption for the VCO. Furthermore, a higher R_p also allows us to layout smaller NMOS's since we then need a smaller g_m value to cancel R_p. To measure the Q of the inductors, we connected a current source to an inductor and swept the frequency to find Z_L. $Q = \frac{\omega L}{R}$ where $Z_L = R + j\omega L$. The inductors in our design are 25 nH each with parasitic R_S ~10 Ω and Q of ~8.4 at 900 MHz. The varactors in our VCO design are PMOS transistors with source/drain connected together to form one terminal and gate as the other. Varactor size is also crucial because the losses in this type of capacitor are quite large and will lower the Q value of the RLC tank, which degrades the phase noise. Therefore, its magnitude is chosen to be a small fraction of the effective tank capacitance, yet still large enough to provide proper tuning range. To make sure that VCO is compatible when integrated in the PLL system, the initial V_{CONT} voltage and output voltage swing need to be considered. To ensure lock acquisition, we set the V_{CONT} to a value close to that which causes the steady state output frequency. Also, the VCO output swing needs to be large enough for the input of the fractional divider input. The following analysis estimates the VCO output swing:

$$\boldsymbol{V_{swing} = I_{mirror} * R_p \ \ where\ \ R_p = R_s * (Q^2 + 1)} \qquad \text{(eq.4)}$$

Our I_{mirror} of 1.8mA achieved the adequate swing of 1.2 V. Also, in order for the output to oscillate, we need $g_m R_p > 1$ We sized the NMOS's for an adequate g_m = 1.5mS. Because the DC level of the output is at 1.56V, our designed swing goes slightly beyond Vdd. However, this does not account for the parasitic resistance of the varactor, which in simulation gave us functional swing of $1.85V_{ppk}$ that lies within the rail tolerances of the divider.

C. Dual Modulus Divider / Prescaler

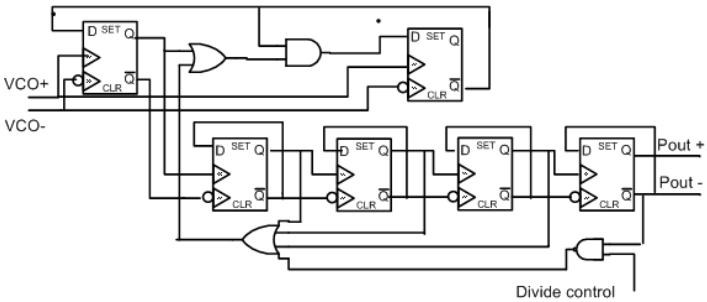

Figure 5: Block Diagram of the Prescaler/DMD

The final block of the synthesizer performs the frequency multiplication for the PLL. Since we must be able to lock onto 124 output frequencies with 200kHz spacings over a 25MHz bandwidth, we need a fractional divider of high resolution. This is typically done with a prescaler and dual modulus divider. However, that has more limited resolution compared to a design which incorporates both blocks in one. Our design dithers by 32/33, and it can generally be shown that the resolution of the synthesizer increases as the N value in N/N+1 increases. It is implemented in current mode logic (CML), which is fully differential and operates faster than CMOS. Also, because it operates on current biasing, less noise is injected on the power rails which, when coupled onto the VCO, causes oscillation jitters and more phase noise. Transistor level design of the main blocks are given below:

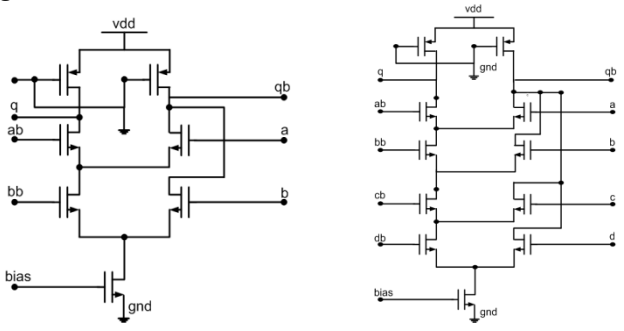

Figure 6: a) AND/OR/NAND gate b) OR4 gate

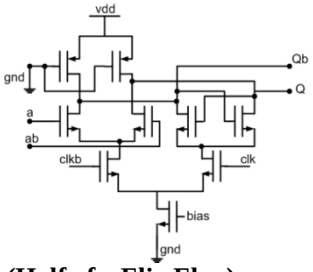

Figure 7: D-latch (Half of a Flip Flop)

The critical parts here are to design the top two flip flops in fig. 5 for fast T_{CQ} and low T_{setup} since they are clocked at the highest frequency of f_{out}. This generally implies using larger bias currents, and was minimized to 50uA in our case. The downside to using smaller currents is the increased phase error at the outputs of the divider caused by increased T_{CQ} delays of each of the registers. By sizing down the signal path transistors in our flip flops, we were able to minimize capacitances, lower T_{CQ} delays, and minimize this phase error. The simulated phase error was around 0.6°. This phase error is another source of phase noise at the synthesizer output. Finally, in integrating this block into the system, the output had to have near rail to rail swing since it feeds into a CMOS PFD. Our output swings from 0.2V – Vdd, which is fine since these values are within V_{thn} and V_{thp}.

III. Main Challenges

A. Design Challenges

The difficult parts of the design came with integrating the PFD/CP with the VCO. This was because the output of the CP (V_{CONT}) needed to be calibrated to center around the linear region of fig.12 for the VCO. This required redesign work and multiple simulations to tune, most of which was performed on the VCO, which was much more flexible to change compared to the PFD/CP.

B. Simulation Challenges

PLL's have a downside of taking massive amounts of time and resources to simulate. We overcame the disk quota issue by running simulations in local /tmp directories, and partly overcame the simulation time handicap by modeling parts of the PLL performance in MATLAB, which is much faster.

C. Layout Challenges

Layout of the digital blocks consisted of standard parts and posed no problem for DRC and LVS. However, L and C passives in the VCO caused LVS issues related to ground connections and netlist mismatches. In the end, the whole design passes DRC, and there were only a few LVS errors pertaining ground connection errors with the VCO passives.

IV. System Level Analysis / Calculations

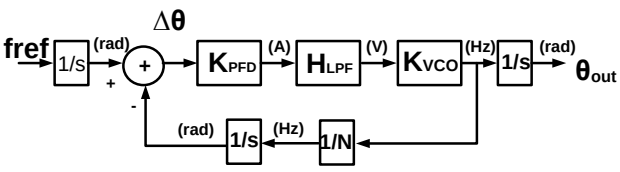

Figure 8: Control System Level diagram of Synthesizer

The closed loop transfer response of the system is modeled by

$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{H(s)_{open\ loop}}{1+\left[\frac{1}{N}H(s)_{open\ loop}\right]} \qquad \text{(eq.5)}$$

where $H(s)_{open\ loop} = K_{PFD}H(s)_{LPF}\frac{K_{VCO}}{s}$

and $H(s)_{LPF} = \frac{1+SRC_1}{s(C_1+C_2(sRC_1C_2)}$

Using simulation values for K_{PFD} and K_{VCO}, the closed loop response is plotted below:

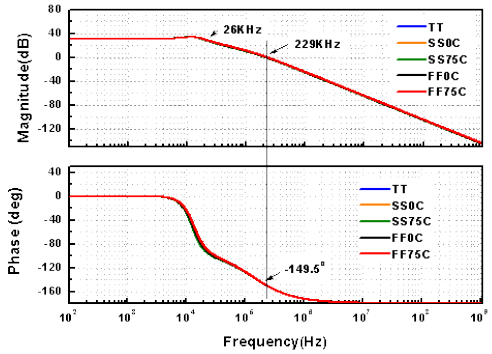

Figure 9: Closed Loop Phase T.F. of the Synthesizer

From fig.9, we can verify that f_{3dB} = 26kHz is relatively consistent with the estimate that the loop BW of a PLL is roughly equal to the cutoff frequency of the LPF, which we designed to be 33kHz. We can also find from the plot that the system is stable, having a phase margin of ~30° at an f_t of 230kHz. With further time, we would also have done matlab analysis on the phase noise of the system introduced by error sources in red in fig.7. This would involved adding an effective V_{NOISE} on top of the V_{CONT} node, the resulting response of which would have been

$$\theta_{out}(s) = \frac{\theta_{ref}(s)K_{PFD}\,H_{LPF}(s)+V_{noise}(s)}{N*s+K_{VCO}\,K_{PFD}\,H_{LPF}(s)} \qquad \text{(eq.6)}$$

An FFT plot of the V_{CONT} node below shows that most of the fluctuation at that node would have been rejected by the low loop BW anyway, a factor that helps the phase noise performance of the system assuming a clean reference input.

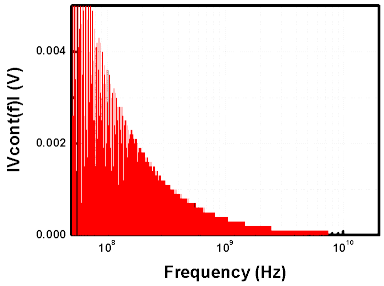

Figure 10: S.S. Spectrum of the V_{CONT} (1.15V at DC)

V. Simulations

Below are some of the key simulations characterizing the synthesizer:

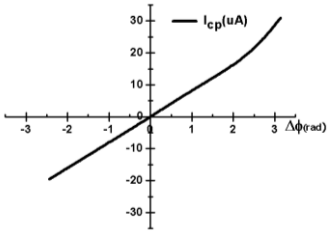

Figure 11: I_{CP} vs. Input Phase Difference (PFD/CP)

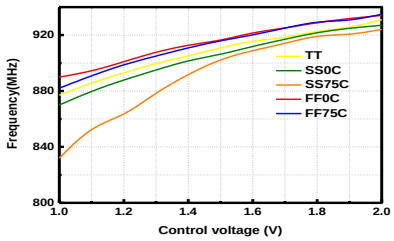

Figure 12: VCO f_{out} vs. V_{CONT} (no osc. At SS75C, low V_{CONT})

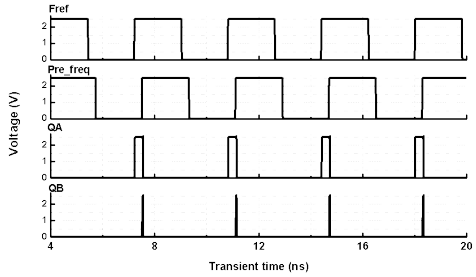

Figure 13: Time Plot of f_{ref}, $f_{feedback}$, and CP Control Pulses

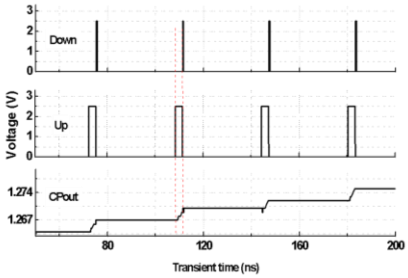

Figure 14: Time Plot of CP Control Pulses and V_{CONT}

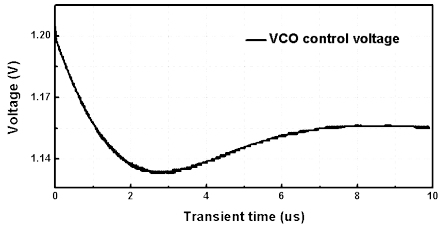

Figure 15: Overdamped Transient Response of V_{CONT}

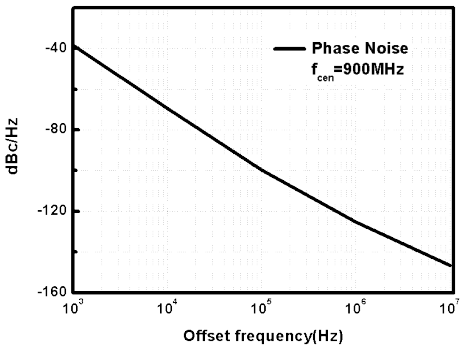

Figure 16: Phase Noise Performance of the VCO

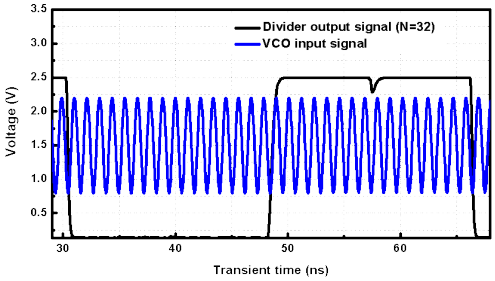

Figure 17: DMD/Prescaler Input and Output

VI. Summary Table

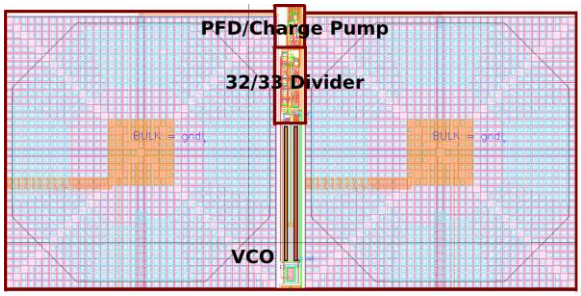

Figure 18: Layout of the Frequency Synthesizer Chip

Overall	**Value**	**Units**
Power	10.27	mW
Phase Noise	(see VCO)	dBc/Hz
T_{SETTLE}	8 (longer as Δf increases)	µs
f_{ref}	27.8	kHz
Loop BW	~ 26	kHz
PFD/CP		
V_{DD}	2.5	V
Power	611 / 457 (PFD/CP)	pW / µW
K_{PFD}	7.76	µA/rad
VCO		
V_{DD}	3.3	V
Power	7.34	mW
K_{VCO}	53.33	MHz/V
Phase Noise	-100 (@100kHz offset)	dBc/Hz
DMD		
V_{DD}	2.5	V
Power	2.47	mW
T_{CQ} (DFF)	160 (loaded)	ps
T_{SETUP} (DFF)	210 (loaded)	ps

Figure 19: Summary of Frequency Synthesizer Performance

VII. Conclusions

Overall, the frequency synthesizer performance was good in many areas, and less satisfactory in others. The power consumption was excellent compared to other papers, although the output was unloaded. The phase noise of the VCO was also excellent, and judging by the V_{CONT} spectrum, the overall phase noise should not be much worse. However, our settling time is longer than desirable, and this can be fixed with changes on parameters such as the loop BW, which was on the low side and hurts stability.

References

[1] K. Waheed, K. Desai, F. M. Salem, "A Low Power Frequency Synthesizer with an Integrated Negative Transconductance LC-tuned VCO", IEEE Xplorer, 2003
[2] C. Lam, B. Razavi, "A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-um CMOS Technology", JSSCC, vol. 35, #5, May 2000.
[3] K. Elserougi, R. Fernando, L. Wei, "Phase Lock Loop Design", Santa Clara University
[4] T. H. Lee, "The Desugn of CMOS Radio-frequency Integrated Circuits", ISBN 0-521-83539-9, 2004
[5] B. Razavi, "Design of Analog CMOS Integrated Circuit", ISBN 0-07-118839-8, 2001
[6] P. Andreani, S. Mattisson, "On the Use of MOS Varactors in RF VCO's", IEEE JSSCC, vol. 35, #6, June 2000
[7] A. Hajimiri, T. H. Lee, "Design Issue in CMOs Differential LC Oscillator", IEEE JSSCC, vol. 34, #5, May 1999.