

A 6.75 – 7.25 GHz Pulse Position Modulation Ultra-Wideband Receiver Front End



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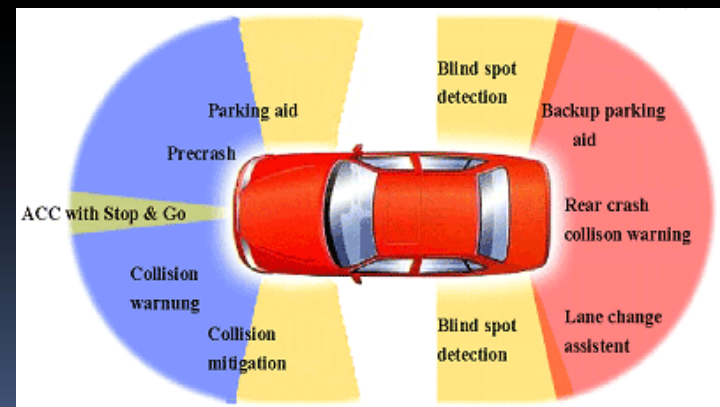
Mark Swiderski

Outline

- **Introduction**
 - Motivation
 - Pulse Position Modulation
- **System Overview**
 - Design Specifications
 - Individual Stage Design
- **Conclusion**
 - Results
 - Design Challenges
 - Questions

Motivation

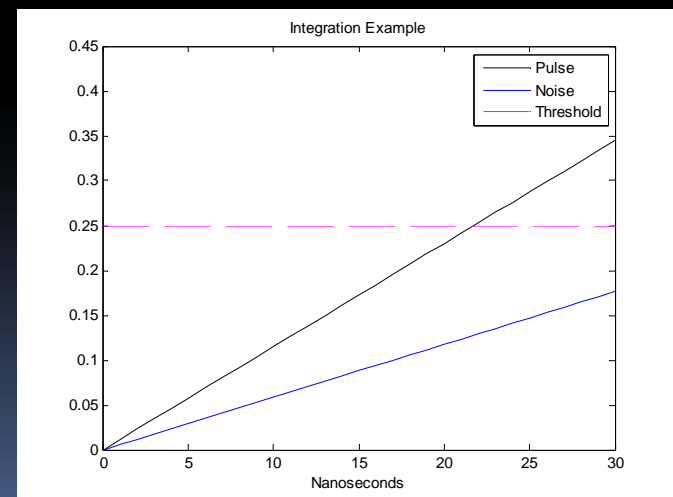
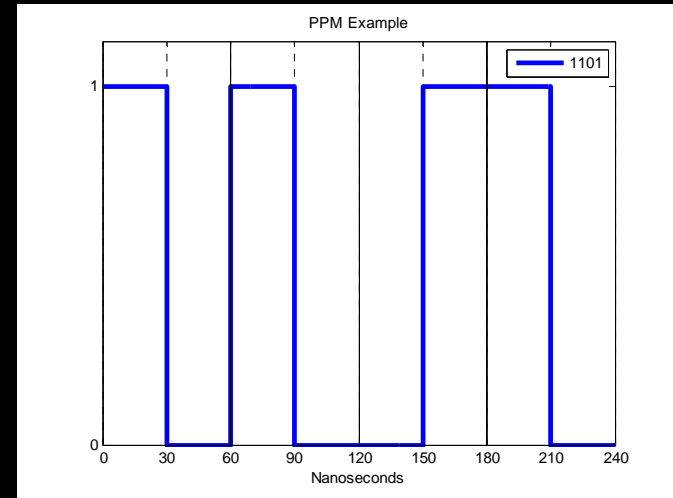
- UWB Communication, WPAN/WLAN
- High Speed/Short Range
- Higher end of UWB band
 - Available in most countries, not just U.S.A.



Images taken from [8] and [9]

Pulse Position Modulation

- Energy detection
 - 2 integration time windows
 - Threshold detection
- Advantages
 - Low Power
 - Low Complexity
- Disadvantages
 - Low Data Rate
 - Sensitive to channel noise



Bandwidth Reduction

- Non-Coherent Energy Detection
 - An optimal Receiver Bandwidth Exists
- Slight degradation in system performance provides:
 - Hardware benefits
 - Low power consumption
 - Better input matching
 - Reduced adjacent channel interference.

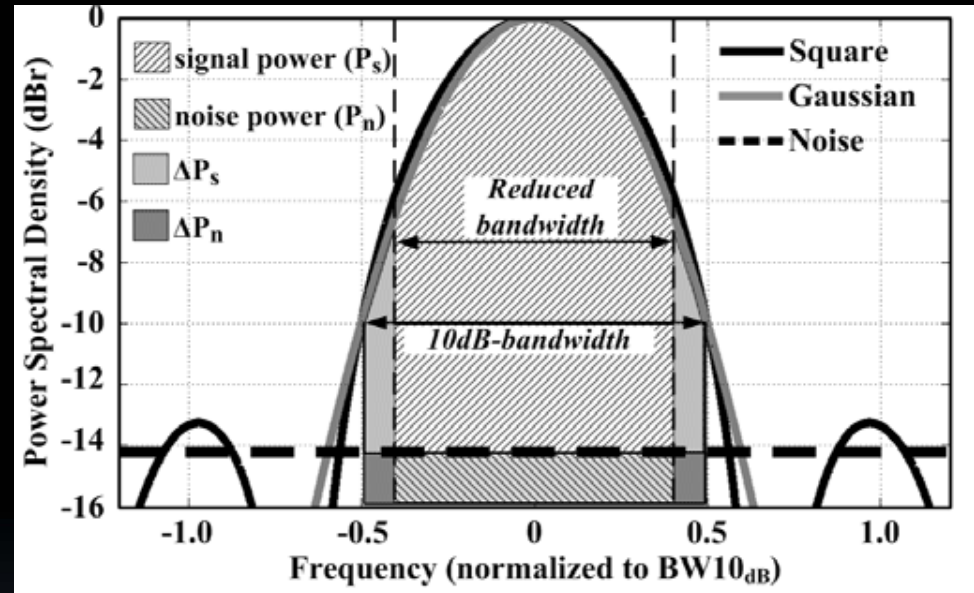
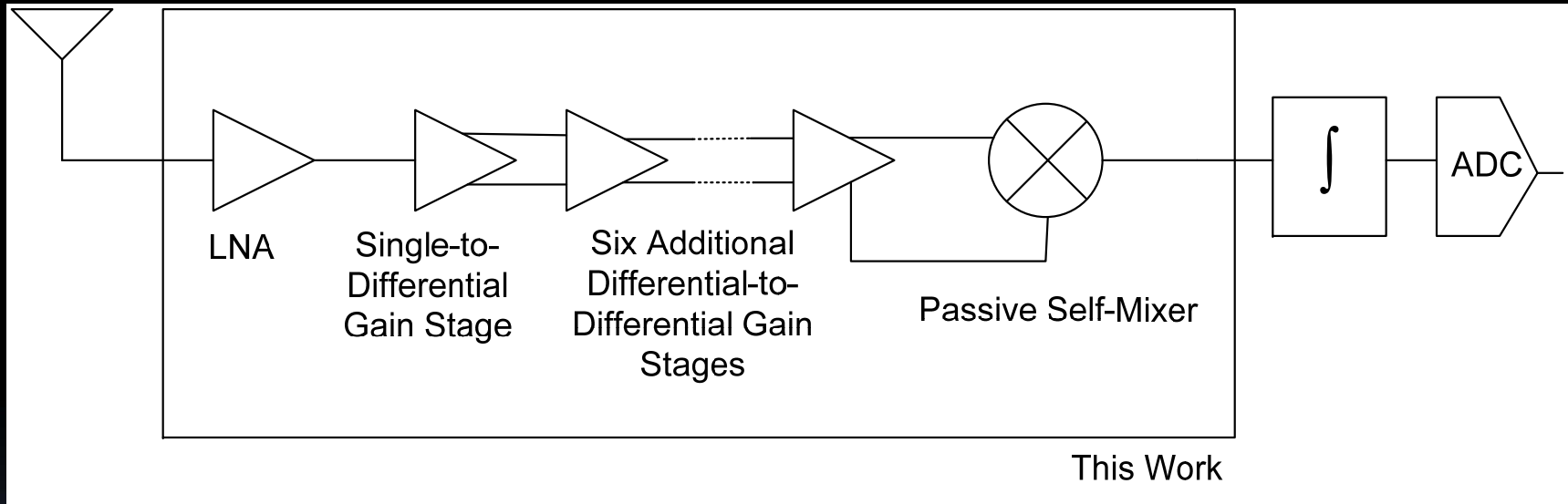


Image taken from [2]

Design Specifications

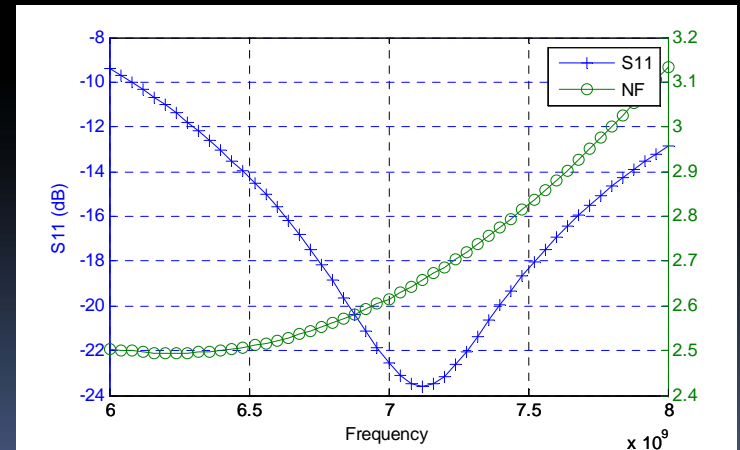
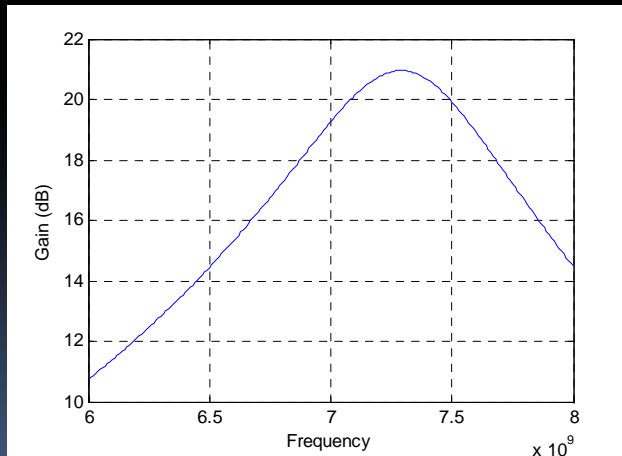
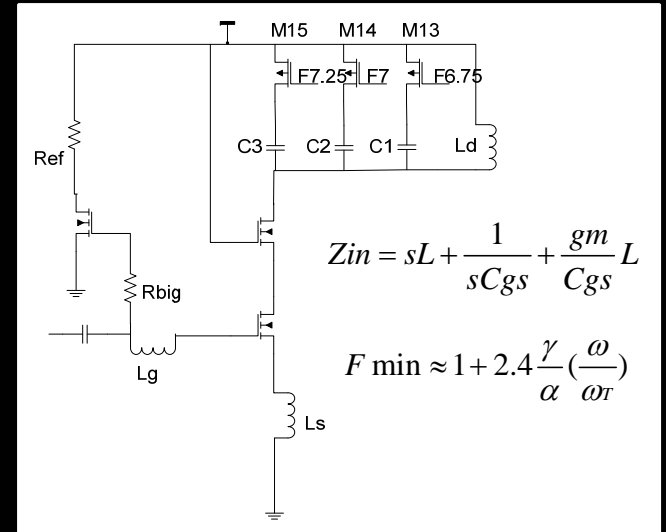
Parameter	Desired
Process	0.13 μm CMOS
Data Rate	16.67 Mbit/s
Supply	1.2 V
Channel Δf	250 MHz
fc Subbands	6.75, 7, and 7.25 GHz
Gain	> 40 dB
NF	< 10 dB
S11	< -10 dB
Power	< 40 mW
Distance	10 m

System Overview



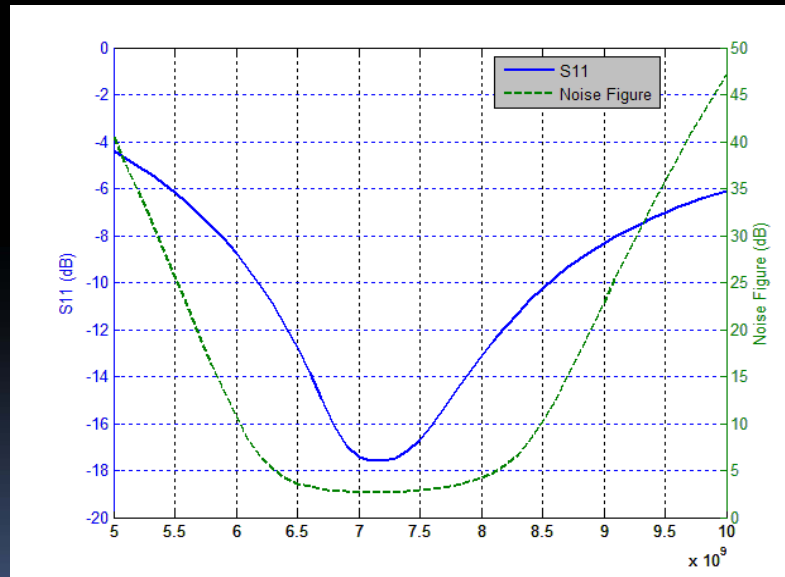
Low Noise Amplifier

- Input Referred P1dB
 - -4.4 dBm
- IIP3
 - 8.5 dBm



Low Noise Amplifier

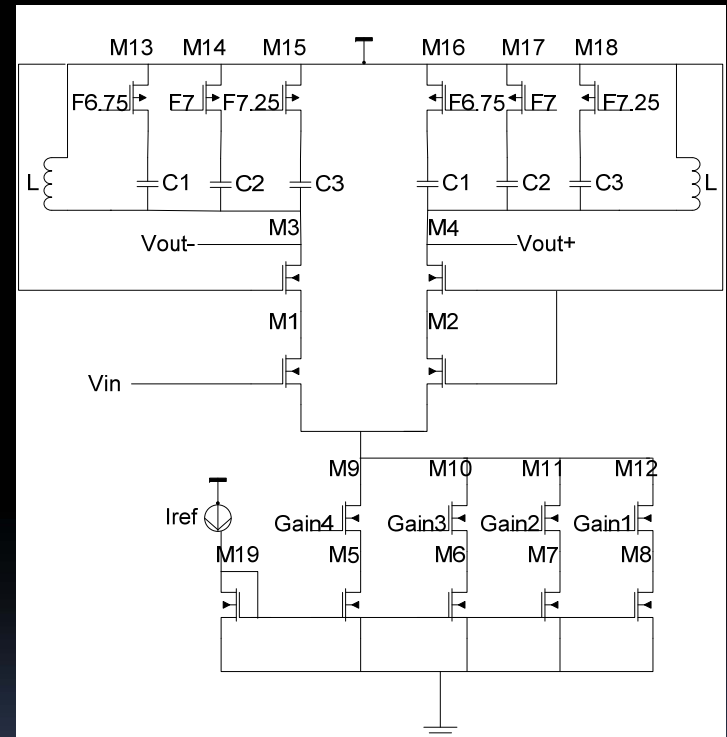
- Overall NF < 2.6 dB
- Overall Return Loss > 15 dB



Noise Figure and S11

Controllable Gain Stages

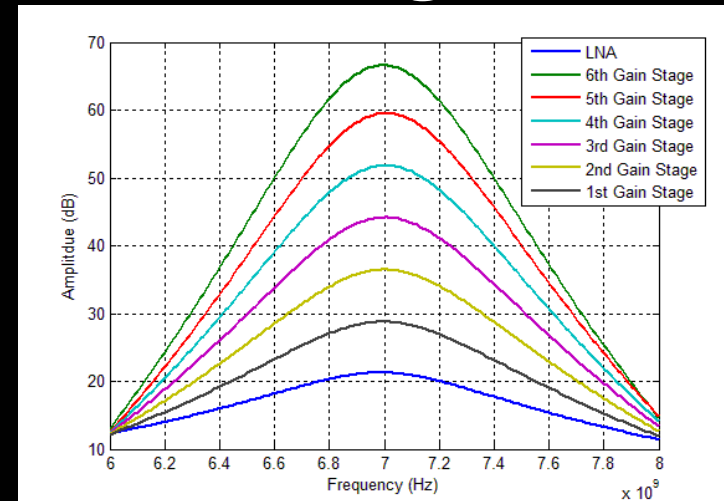
- Design Strategy
 - Simple diff amp with LC tank load
 - Used gm/W vs. I/W plots to optimize between power, gain, and noise figure
 - Added cascode to increase isolation between stages
 - Single-to-differential conversion done in 1st stage



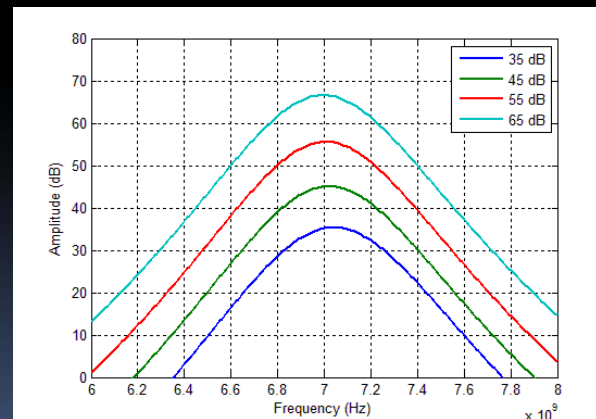
First gain stage with switchable gain and f_0

Controllable Gain Stages

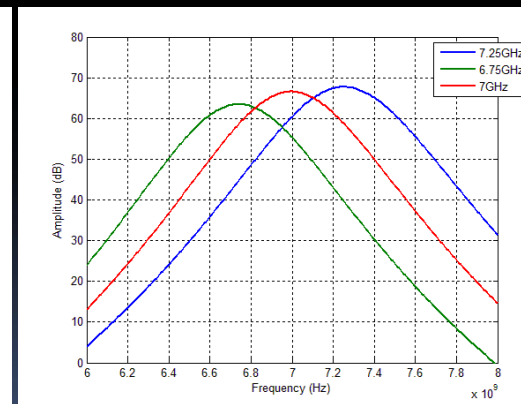
- Switchable load on all stages
 - Need for high overall Q
 - Optimize switch sizing
- Switchable gain on first stage only
 - Switching affects f_0
 - First stage relatively wideband



Overall Gains



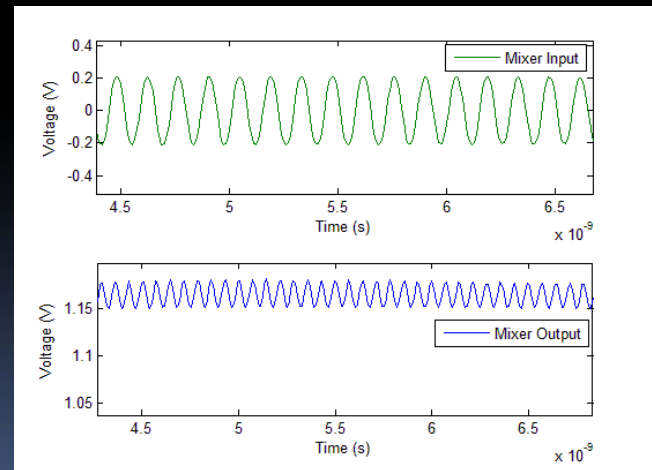
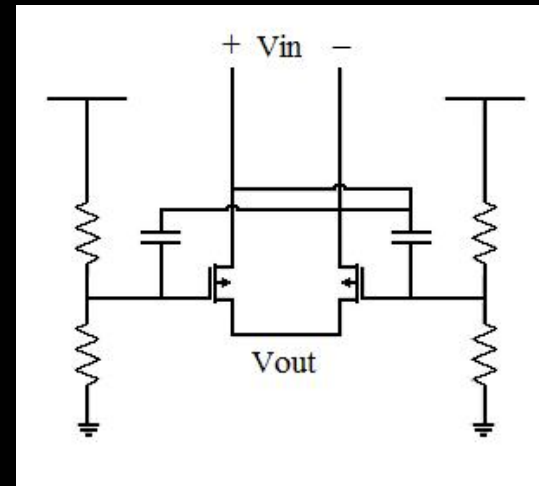
Proper Functionality of Gain Control



Proper Functionality of Channel Selection

Self-Mixer

- Voltage Controlled Resistance.
- Biased near V_{th}
 - Achieves best swing of resistance
- Passive
 - Very Low Power
 - High NF and Conversion Loss
- Differential to Single-Ended Output



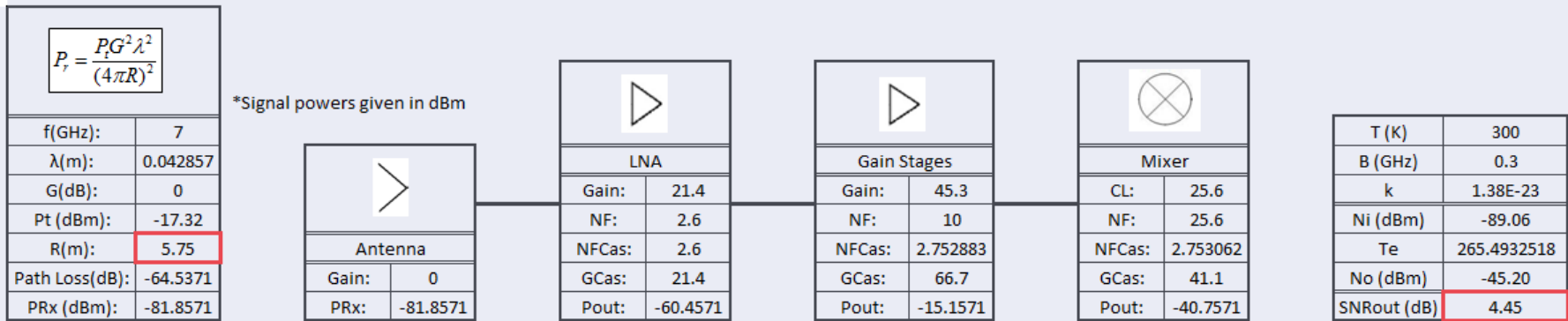
Self-Mixer Input and Output

Results

- We can now find the approximate range for Non-coherent PPM with BER of 10^{-3} [1]

$$\frac{E_b}{N_0} = 17dB$$

$$SNR_{out} = \frac{E_b}{N_0} - 10\log(BW) + 10\log(R) \approx 4.45dB$$



Results

Parameter	This Work	Desired	Li, Xia, Huang	Fred Lee Thesis
Process	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	90nm CMOS
Data Rate	16.67 Mbit/s	16.67 Mbit/s	-	16.67 Mbit/s
Supply	1.2 V	1.2 V	1.2 V	0.65 V
Die Size	0.869 mm x 3.83 mm	-	1.1 mm x 1.5 mm	1mm x 2.2mm
Channel Δf	300 MHz	250 MHz	> 250 MHz	500 MHz
fc Subbands	6.75, 7, and 7.25 GHz	6.75, 7, and 7.25 GHz	3.4, 3.9, and 4.4 GHz	3.4, 3.9, and 4.4 GHz
Gain	40 dB	> 40 dB	22 dB	40 dB
NF	2.6 dB	< 10 dB	3.3 - 4 dB	8.6 dB
S11	< -15dB	< -10 dB	< -10 dB	-
Power	34.4 mW	< 40 mW	21.6 mW	-
Distance	6m	10 m	-	7m

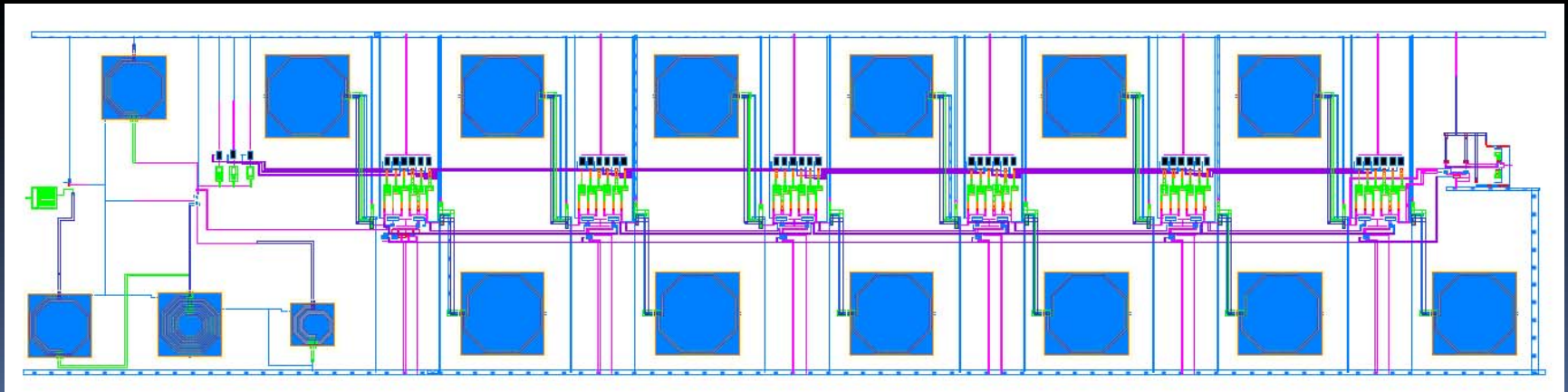
Layout

- 0.869 mm x 3.83 mm
- Inductors spaced 1 diameter apart to reduce coupling

LNA

Controllable Gain Stages

**Buffer and
Self-Mixer**



Design Challenges

- Upper Band Channel Selection
 - High Q, Narrow Bandwidth
- Center Frequency Tuning
- Channel and Gain Switches
- Mixer Characterization
- Die Size

Conclusions

- Specifications reasonably met or exceeded
 - Very low noise figure
 - Good input matching, gain, and BW
- Large die size
- Future Work
 - Differential Inductors
 - Higher order filters
 - Fewer Gain Stages

Questions



References

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5. T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed., Cambridge University Press, 2003.
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7. W. Li, L. Xia, Y. Huang and Z. Hong, "A 0.13um CMOS UWB Receiver Front-End Using Passive Mixer," *Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference*, pp. 288-291.
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