A 6.75 – 7.25 GHz Pulse Position Modulation Ultra-Wideband Receiver Front End

David DuRussel, Osama Khan, and Mark Swiderski

***Abstract*—This paper describes a three channel ultra-wideband receiver front end for PPM communication designed in a 0.13µm CMOS process. The architecture is based on a non-coherent impulse-radio energy detection scheme. The three channels have center frequencies in the upper end of the UWB spectrum at 6.75, 7, and 7.25 GHz. The channel bandwidth is approximately 300 MHz. Channel selection is done using switchable filter loads. The overall gain is also controllable. The receiver dissipates 34.4 mW with a 1.2 V supply.**

***Index Terms*—UWB, pulse energy detector, LNA, self-mixer**

I. Introduction

Although the concept of ultra-wideband communication has been known and used for several decades, it is currently being re-visited by the integrated circuits community as a viable high-speed, short-range wireless link technology. Ultra-wideband signals, with their large bandwidth, propagation characteristics and high timing resolution, add special advantages to wireless communication that make it suitable for applications such as WPAN/WLAN, wireless USB & multimedia, locationing/tagging and biomedical imaging. At the same time UWB poses interesting design challenges, especially in the upper end of the spectrum, including narrowband channel selection and wideband input matching. The non-coherent energy detection architecture relaxes linearity requirements but makes the receiver sensitive to noise [2], increasing the need for a low noise figure.

The paper is organized as follows: Section II describes the system level architecture of the receiver, section III covers the analysis and design of the circuits used in the receiver, section IV presents simulated results and section V presents conclusions.

II. System Level Architecture

Figure 1 shows a block diagram of the receiver, which has the same architecture as that presented in [1]. It consists of an LNA, cascaded gain stages, and a passive self-mixer. Because of the passive nature of the self-mixer, the amplitude of the mixer's input signal must be relatively large in order for it to correctly perform the mixing operation, making it necessary to add cascaded gain stages after the LNA. The first gain stage also performs single-to-differential conversion to decrease the effect of common-mode disturbances in later stages (i.e. power supply fluctuations, external noise coupled to wires, etc.). The LNA and gain stages have LC tank loads that are tunable by switching in different capacitances using three external digital inputs, providing channel selection and the required filtering at each channel to achieve a fractional bandwidth of around 4.3%. The overall gain of the system is also tunable by controlling the bias current of a gain stage using four external digital inputs. This allows the gain to be varied depending on the incoming signal, preventing the receiver from becoming saturated.

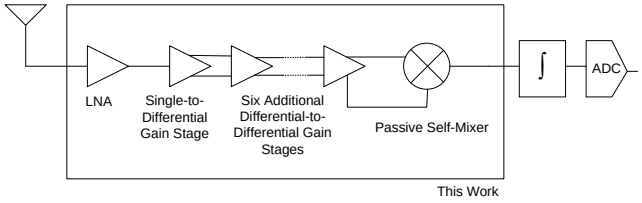

Figure 1: Block Diagram of UWB Receiver

III. Circuit Analysis and Design

A. LNA

The complete schematic for the Low Noise Amplifier is shown in Figure 2. The LNA is almost always the first stage in a receiver chain. Its main function is to provide adequate gain to suppress the noise of the subsequent stages while adding minimum amount of noise to the signal. The other requirements for the LNA in a typical receiver system are linearity and input match. Recently, minimum power consumption has also become one of the critical requirements of LNA.

From various LNA topologies available, the degenerated common source amplifier is selected for its superior noise performance and adequate input match bandwidth.

The design procedure is based on power constrained noise optimization method [5]. The input impedance seen at the gate of a degenerated common source LNA is given by (1) and minimum achievable noise figure under power constraint is given by (2).

$$Zin = sL + \frac{1}{sCgs} + \frac{gm}{Cgs}L \qquad (1)$$

$$F\min \approx 1+2.4\frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right) \quad (2)$$

As can be seen from (1) the input impedance is equivalent to a series RLC circuit. The real part of this impedance is made equal to the input source impedance to provide the required input match. In order to have one extra degree of freedom to select the resonant frequency of the series RLC circuit, an additional inductance is added in series with the gate of the common source amplifier.

Since the load is a switchable band-pass filter, a cascode device is added to the degenerated common source device to isolate the input and output load resonant circuits. The size of the cascode device is chosen to be equal to that of the common source device.

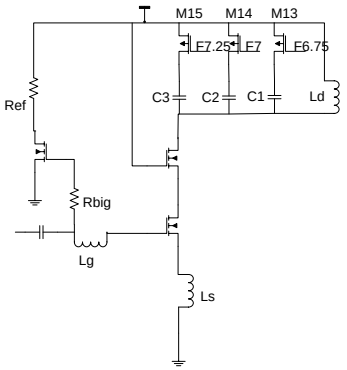

Figure 2: Cascoded Common Source LNA with Inductive Degeneration

The total power consumption of the LNA is 5.8 mW. The achieved gain over the three channels is greater than 20 dB, input return loss greater than 15 dB and the worst noise figure over the three channels is less than 2.5dB.

B. Gain Stages

The complete schematic of the first gain stage is shown in Figure 3.

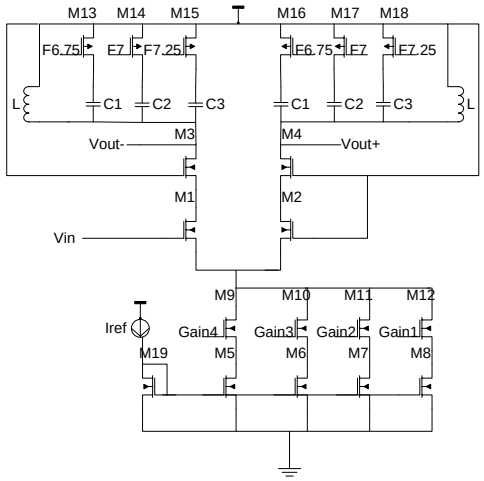

Figure 3: First Gain Stage

The subsequent gain stages are the same except they do not have switchable current sources for gain control and the negative input is not shorted to Vdd.

The initial design for these gain stages was a simple differential pair with an LC tank load, providing a gain of $|A_v| = g_{m1,2} \cdot R_P$, where $R_P = R_S \cdot \left(Q_L^{\,2}+1\right)$, with R_S and Q_L being the series resistance and Q of the inductor respectively. The design methodology made use of plots of current density vs. g_m density, which were created for devices of different lengths. By choosing a current density near the knee of these plots, a high g_m density is achieved with a minimum amount of current density, providing a larger gain without excessive power consumption. Once the current density was chosen, the device size was chosen based on the specification for power consumption in these stages. The noise figure was then calculated and this process was repeated to optimize between power consumption, gain and noise figure. The first gain stage also needed to provide single-to-differential conversion. Several techniques were considered [3][4], but in the end, the conversion was achieved by simply AC grounding the negative input of the differential pair. This provides a simple and reasonable S2D conversion but at the expense of gain, which is reduced by a factor of ½, and any errors in this S2D conversion would be corrected as the signal passes through additional differential amplifiers.

When the stages were cascaded, it was discovered that the load of each stage was affecting the load of the previous stage, causing a change in center frequency as well as very high load Q's which led to instability and oscillations. This interaction was due to the C_{gd} capacitors of M1 and M2 and the Miller effect. To eliminate this problem, cascode devices (M3 and M4) were added in order to reduce the effect of C_{gd} and isolate the loads of each stage.

In order to achieve a bandwidth of only 300 MHz around the center frequencies desired, a very high Q was required. This could not be achieved by adjusting the values of L and C as the size of L would need to be impractically small. Therefore, each gain stage has an LC filter tank load and the cascade of these filters provides the desired bandwidth. Three switchable channels at 6.75, 7, and 7.25 GHz are achieved by including three capacitors in the LC tank of each gain stage that can be switched in or out using PMOS switches. There is a tradeoff between the on resistance of the switch and the parasitic capacitances associated with it. Therefore the PMOS switches were sized large enough to increase the on resistance but small enough to provide good isolation by not increasing the parasitic capacitive paths.

Gain control is implemented in the first stage by allowing different current sources to be switched in using NMOS switches. Using this technique, four choices of gain (35, 45, 55, and 65 dB) can be selected while the center frequency fluctuates only slightly.

C. Passive Self-Mixer

The complete schematic of the self-mixer is shown in Figure 4.

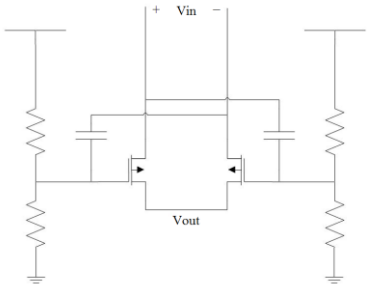

Figure 4: Self-Mixer

Since the receiver uses non-coherent energy detection, it only needs to detect whether or not a signal is present. Through the use of a self-mixer we can convert our signal down to baseband and integrate the DC component of the output for energy detection. If no signal is present, only noise will be integrated. To this end, we decided upon using a passive, single balanced, and differential to singled-ended type mixer [1]. The passive design will allow for low power and the single ended output will be ideal for signal integration. This is a commutating mixer that is biased such that each transistor operates as a variable resistor. To facilitate the low conversion loss and high channel resistance swing, the transistors are biased close to their threshold voltage [1]. Since the LO port is fed the RF signal, the output will have components at DC and twice the RF signal. The harmonics produced by this down conversion will be filtered out in the integrator.

Linearity and gain of the mixer hold less importance since we are only detecting energy. Noise figure requirement for the mixer is also not stringent as there is sufficient gain before the mixer to suppress its noise. The most important design consideration was to keep the mixer conversion loss low enough to produce adequate SNR at the output to be eventually detected by the ADC.

IV. Results

A summary of the important specifications are given in the link budget of Figure 9 as well as Table 1.

Figure 5 shows the proper functionality of the channel selection and Figure 6 shows the proper functionality of gain control.

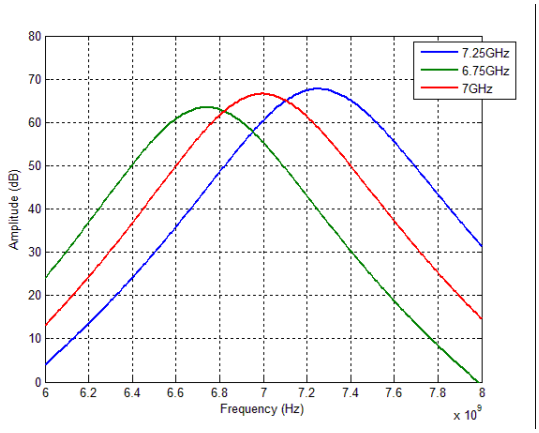

Figure 5: Proper Functionality of Channel Selection

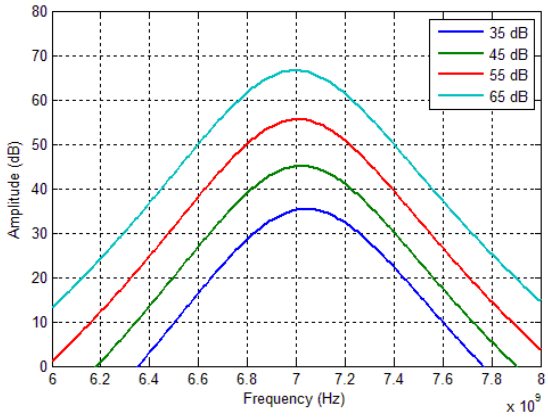

Figure 6: Proper Functionality of Gain Control

Figure 7 shows both the noise figure and S11. As can be seen, input matching and low noise figure (2.7 dB) is achieved across the entire 6.75 to 7.25 GHz bandwidth.

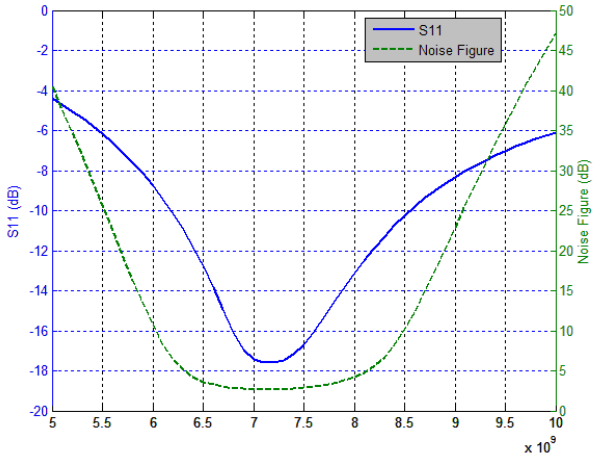

Figure 7: Noise Figure and S11

Figure 8 plots the transient input and output of the mixer, showing correct mixer functionality.

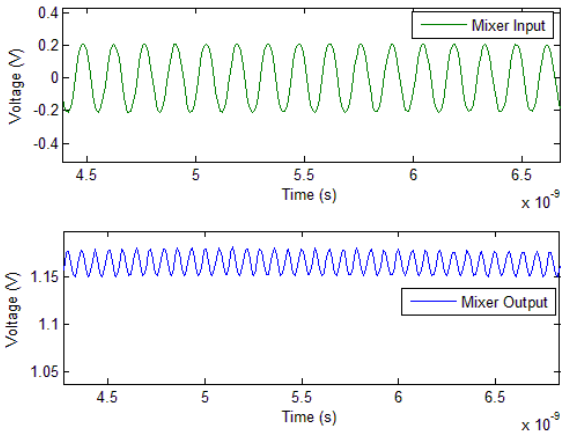

Figure 8: Self-Mixer Input and Output

For non-coherent PPM, a BER of 10^{-3} requires an EB/No of 17 dB. The required SNR at the output is given by SNR (dB) = Eb/N0 – 10log BW + 10log R [1].

From this equation we find that we require an SNR of at least 4.45dB to detect a signal. From the link budget analysis in Figure 12, we find that our maximum transmission range will be approximately 6 m.

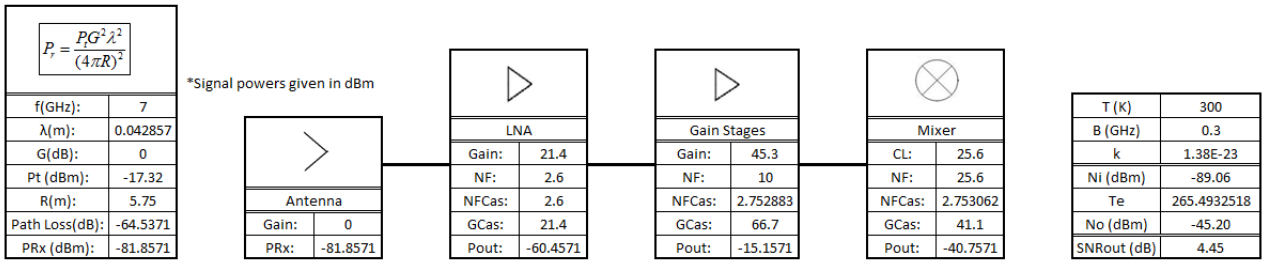

Figure 9: Link Budget Analysis

Parameter	This Work	Desired	[7]	[1]
Process	0.13 µm CMOS	0.13 µm CMOS	0.13 µm CMOS	90nm CMOS
Data Rate	16.67 Mbit/s	16.67 Mbit/s	-	16.67 Mbit/s
Supply	1.2 V	1.2 V	1.2 V	0.65 V
Die Size	0.869 mm x 3.83 mm	-	1.1 mm x 1.5 mm	1mm x 2.2mm
Channel Δf	300 MHz	250 MHz	> 250 MHz	500 MHz
fc Subbands	6.75, 7, and 7.25 GHz	6.75, 7, and 7.25 GHz	3.4, 3.9, and 4.4 GHz	3.4, 3.9, and 4.4 GHz
Gain	40 dB	> 40 dB	22 dB	40 dB
NF	2.6 dB	< 10 dB	3.3 - 4 dB	8.6 dB
S11	< -15dB	< -10 dB	< -10 dB	-
Power	34.4 mW	< 40 mW	21.6 mW	-
Distance	6m	10 m	10m	7m

Table 1. Performance Summary Table

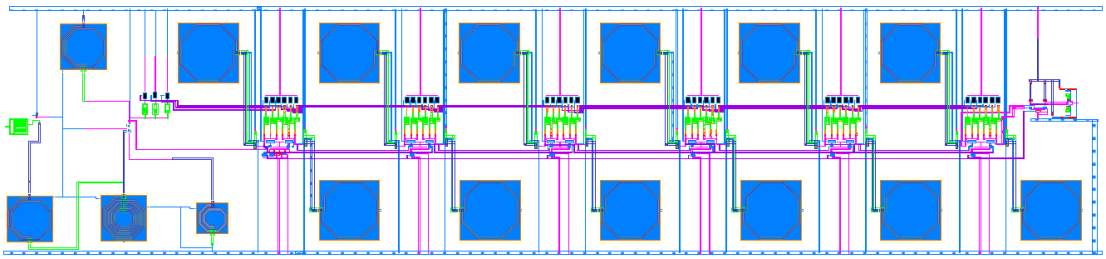

Figure 10. Receiver Layout

The layout is both DRC and LVS clean, aside from errors in using different metal types (4-1 and 3-2).

I. Conclusions

A three-channel ultra-wideband receiver front end designed in a 0.13µm CMOS process has been presented. It operates in the upper end of the UWB spectrum, making it unique from other recent implementations [1,6]. The main design challenges have been discussed and simulated results have been presented. We have achieved a low noise figure, good input matching, and high gain across our bandwidth of interest. We have also implemented channel selection and gain control. The overall power dissipation is 34.4 mW with a 1.2 V supply. Future work could reduce the number of inductors used and thus the overall area by implementing higher order filters as the loads of each stage. This would provide the desired Q with less reactive elements and reduce the number of cascaded gain stages needed.

References

[1] F. S. Lee, "Energy Efficient Ultra-Wideband Radio Transceiver Architectures and Receiver Circuits" PhD Thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, 2007.

[2] J. M. Almodovar-Faria and D. D. Wentzloff, "Optimal Filter Bandwidth for Non-Coherent UWB Receivers," Unpublished.

[3] G. Palmisano and S. Pennisi, "CMOS single-input differential-output amplifier cells," *Circuits, Devices and Systems, IEE Proceedings*, 6 June 2003, pp. 194-198.

[4] K. Han, L. Zou, Y. Liao, H. Min and Z. Tang, "A Wideband CMOS Variable Gain Low Noise Amplifier Based on Single-to-Differential Stage for TV Tuner Applications," *Solid-State Circuits Conference, 2008. A-SSCC '08. IEEE Asian,* 3-5 Nov. 2008, pp. 457-460.

[5] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed., Cambridge University Press, 2003.

[6] Raúl Blázquez, "Ultra-wideband Digital Baseband", PhD Dissertation, Massachusetts Institute of Technology, 2006.

[7] W. Li, L. Xia, Y. Huang and Z. Hong, "A 0.13um CMOS UWB Receiver Front-End Using Passive Mixer," *Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference*, pp. 288-291.