# Low Area Dual-band LNA with Active Inductor for GSM applications

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***Abstract*—A dual-band (880/1960MHz) LNA with active inductor suitable for GSM applications is presented. LNA with common source topology with inductive degeneration is known to have the best noise figure. However, inductors take a huge area on silicon, which decreases the yield of a wafer. The total number of inductor can be reduced by using parasitic resistance of inductor and active inductors while retaining power matching and low noise. This greatly reduces the total area, significantly reducing the unit cost of each LNA. An integrated switching capability between the two bands is also exploited. It can remove the necessity for an off-chip switch.**

## I. Introduction

AN increasingly important factor in the design of integrated RF front-ends for cell phones is reducing the unit cost. The cost can be significantly reduced by making the die smaller, yielding more chips for the same wafer fabrication effort. This project targets a low-cost, implementation of a low noise amplifier designed to operate in the popular cell phone bands of GSM-850 and GSM-1900, specified in [1]. To reduce the area, and hence the cost, the number of inductors has been reduced by replacing the load inductors with active inductors. An overview of the performance results are given in Table 1.

## II. Circuit Design

To realize narrow bandwidth and low noise figure, both passive and active inductors are used. Active inductor cannot be used at the input of LNA since it is noisy and increases total noise figure greatly where gain is high. Passive inductor can be removed totally from this circuit by using a feedback resistor as in [2]; however, that technique widens the bandwidth and can also increase noise.

The two inputs of the LNAs must share an input connection, causing the input impedance of each LNA to affect the other. This makes input impedance matching difficult and complicated while it helps reducing the total number of inductors. First, each LNA's input is roughly adjusted alone and then tuned with the other one connected.

For the gain, two LNAs have the same structure modified from [3], and can be designed in the same way.

The GSM-850 band mobile receive frequency is actually centered at 880MHz, and the GSM-1900 band receive is centered at 1960MHz, so they are designed for those frequencies.

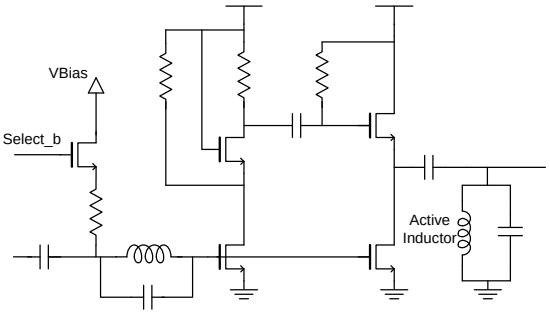



Fig. 1. LNA for 880MHz GSM band

### A. LNA for 880MHz

#### 1) Input Impedance (S11)

The schematic for the GSM-850 band LNA is shown in Fig. 1. A band selection switch turns off LNA for 1960MHz by reducing gate bias voltage to zero, and this makes the Cgs of the first gate in this LNA zero. Therefore, the input path into LNA for 1960MHz can be considered to be floating at the end where the gate exists. In reality, it's not totally disconnected and parts after the first NMOS affect the input matching, but the effect was found to be minimal. Considering the path to the low-frequency LNA, the inductance is set to cancel the capacitance of dc block capacitor and the input transistor's Cgs at 880MHz. The real part of the input impedance comes from the internal resistance of RF inductor. It was measured to be over 30Ohm since the inductor is large at this frequency, which can lead to S11 below -10dB. However, these inductor and capacitors interfere with the other LNA at high frequency, and increase NF for 1960MHz. To cancel out this effect, a very small capacitor is connected to the inductor in parallel. This will be explained in details later in high frequency LNA part.

#### 2) Gain (S21)

This LNA is configured with two stages. The second stage is source follower, thus it has gain of 1 and most gain comes from the first stage which is cascode common source amplifier. In most of this configuration, total gain is defined as $g_mR$, and $g_m$ comes from the first NMOS. However, bias current for the first stage is already fixed for input matching, and changing $g_m$ is difficult here. Therefore only R is determined to generate S21 over 10dB, which causes another problem. Changing R affects dc operating voltages, and transistors can fall into linear region. To prevent this, another resistor is introduced in the intermediate point in cascade structure to steal current into upper NMOS in order to decrease voltage drop at load. This not only guarantees saturation of both NMOSs, but also hardly changes the equation for total gain if an added resistor is well

determined.

### B. LNA for 1960MHz

Fig. 2 shows the schematic for the higher frequency band LNA.

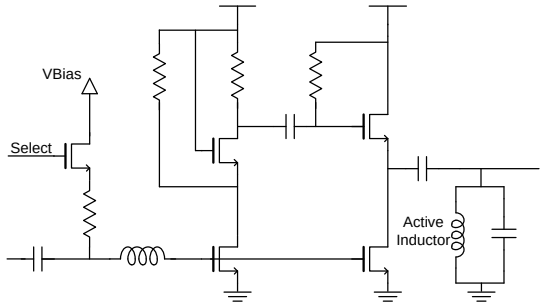



Fig. 2. LNA for 1960MHz GSM band

#### 1) Input Impedance (S11)

Like the lower frequency LNA, LNA for 1960MHz is input matched without considering the other one. But components in LNA for 880MHz are large, and this can cause resonance with small parasitic capacitance in the input path of LNA for 1960MHz. In simulation, there was a glitch in NF around 2GHz which was caused by the large inductor for the lower frequency LNA. To reduce this effect, a small capacitor is connected in parallel in order to resonate with that inductor at 1960MHz. Therefore, the inductor in the other input path cannot have any effect on the higher frequency LNA. This small capacitor in LNA for 880MHz doesn't have significant effect at lower frequency since it is connected in parallel with inductor. The inductor of LNA for 1960MHz is sized in the same way to cancel out capacitors. Here, the inductor is small, and thus parasitic resistance is also small. This is inefficient to match 50Ohm. Back to LNA for 880MHz, even though inductor is in resonance with a capacitor, the parasitic resistance of the inductor still exists. According to Q of inductor, the resistance into resonator changes, but it is clear that it increases. And two parallel paths into two LNAs having complex number input impedances determine the total input impedance at 1960MHz. By fine tuning of components, S11 at 1960MHz can be lowered below -10dB.

#### 2) Gain (S21)

The gain of LNA for 1960MHz has the same equation as the lower frequency one except the value of parameter.

### C. Switching Logic

A switching circuit is essential to realize only one set of input and output ports for the dual band LNA. This also makes it possible to save power by putting the unused LNA into an idle state. Furthermore, good design of switching circuitry makes input impedance matching easier. The primary components of the switching circuitry are shown in Fig. 3.

#### 1) Bias Voltage Controller

The DC bias voltage of NMOS causes DC current flow into both common source amplifier and source follower. This current should be cut off when one of the LNAs is not used.

TABLE 1. PERFORMANCE SUMMARY

| Parameter | Select GSM-850 | Select GSM-1900 |
|---|---|---|
| Center freq. | 906.1 MHz | 1888Mhz |
| S11 | -15dB | -10.69dB |
| S21 | 29.86dB | 12.74dB |
| NF | 2.92dB | 2.88dB |
| 3dB-BW | 85.2MHz | 905MHz |
| P1dB | -0.5dB | 1.995dB |
| IIP3 | -12.71dB | -14dB |
| Power | 13.27mW | 12.97mW |
| Area | 0.301 $mm^2$ | |

For this, NMOSs are used to switch on and off the current into bias voltage generator according to an external switching signal 'Select' or 'Select_b'. Bias voltage is generated from an external bias current by feeding it into a diode connected NMOS. If the bias current is cut off by a switch, bias voltage is set to 0V. The generated bias voltage is switched again right before being fed into LNA to prevent interference.

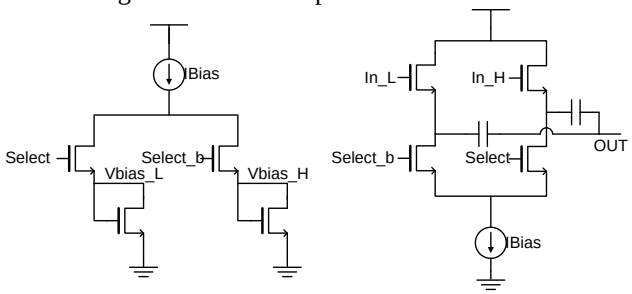



Fig. 3. (a) Bias voltage Controller (b) Selector

#### 2) Selector

When an LNA is in and idle state it still contributes noise at the output, and this should be totally cut off. Two source followers are connected to each LNA, and the bias current into the source followers is steered by selecting signals. This helps prevent one LNA output from affecting the other one.

### D. Active Inductor

In order to get higher gain and narrower bandwidth, each band of the LNA is loaded with a resonant circuit. Typical resonant LC tanks use a spiral inductor; however, these are large and have relatively low quality factors due to the series resistance and the loss due to eddy currents induced in the substrate. The inductance in this design is generated using an active inductor to save area. Other alternatives include using a discrete off-chip inductor or the parasitic inductance of bond wires. Discrete inductors take up a large amount of space, which is very limited in cell phones, and the inductance may not be accurate after taking the effects of packaging and other parasitics into account. The accuracy can be even worse using solely the bond-wire inductance due to variations in wire length and curvature unless a very repeatable packaging process is used which would increase manufacturing time and cost.

The active inductor circuit consists of relatively few components in order to reduce the number of noise generators. The basic topology consists of a gyrator which is used to convert the parasitic $C_{gs}$ capacitance to an inductance, as proposed in [4]. Simple gyrators can be realized as a pair of

back-to-back amplifiers. Here, a cascoded common source amplifier and a source follower are used. The cascode configuration is used to reduce the effective series resistance.

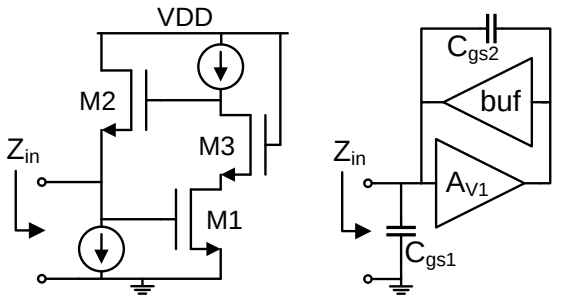



Fig. 4. (a) Transistor-level gyrator (b) Model for analysis

The transistor-level configuration is shown in Fig. 4(a) and an equivalent schematic for analysis is shown in Fig. 4(b), where $A_{V1} \approx g_{m1}g_{m3}r_{o1}r_{o3}$ is the gain of the M1-M3 cascode stage, and $A_{V2} \approx 1$ is the gain of the M2 source follower buffer stage. The input impedance of this circuit can be derived (neglecting gate-to-drain capacitances) as Eqn. 1.

$$Z_{in} = \frac{1}{sC_{gs1}} \parallel \frac{1 + sC_{gs2}r_{o1}}{(1 + g_{m1}r_{o1})(g_{m2} + sC_{gs2})} \qquad (1)$$

This expression for $Z_{in}$ can be equated to the expression for the impedance of a parallel RLC tank with series resistance in the inductor depicted in Fig. 5.

The equivalences relating the gyrator impedance to the passive circuit are derived in [5]. The most important parameters are the inductance and series resistance, calculated using Eqns. 2 and 3.

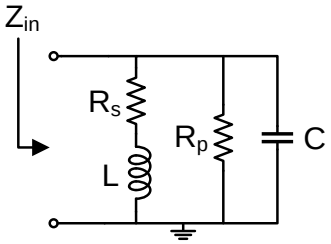



Fig. 5. Passive circuit with equivalent input impedance to gyrator

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}} \qquad (2)$$

$$R_s = \frac{1}{g_{m1}g_{m2}r_{o1}r_{o3}g_{m3}} \qquad (3)$$

Decreasing the $R_s$ is desirable in order to achieve a high quality factor, enabling higher gain and narrower bandwidths.

## III. Simulation

### A. Input Impedance Matching and Gain

S-parameter simulations were performed to verify the correct behavior of input impedance matching (to 50Ω) and gain. The simulation results are shown in Fig. 6. Note that two sets of $S_{21}$ and $S_{11}$ data are simulated for different values of the band select signal, verifying that the signal correctly disables gain through the other band and enables gain for the selected band.

### B. Noise Figure

The noise figure was also measured and is shown in Fig. 6. The graph shows the noise figure around the bands of interest.

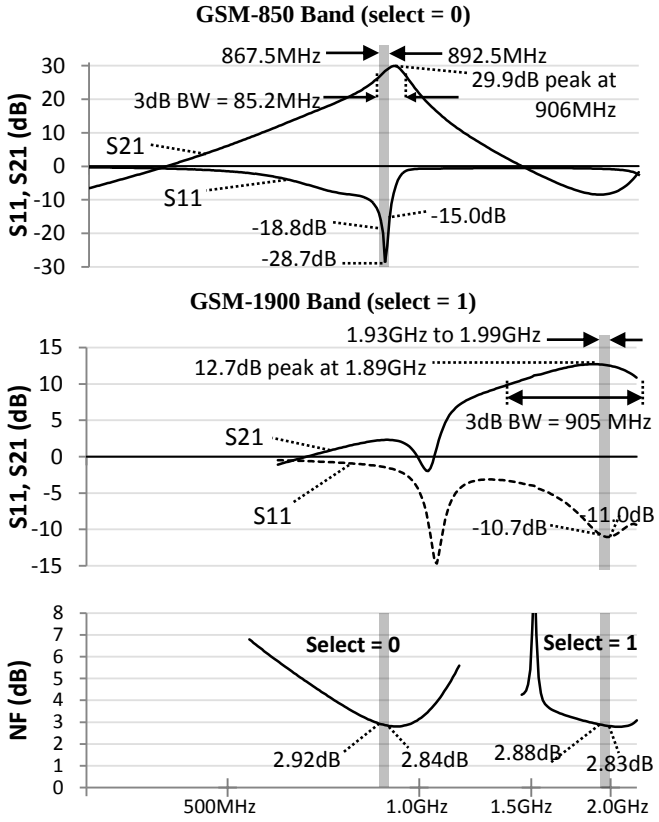
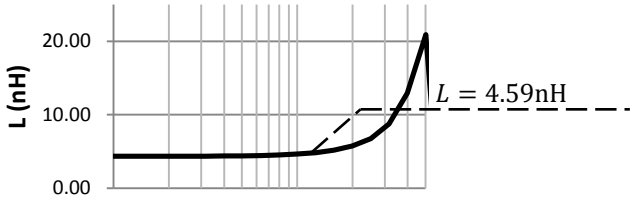



Fig. 6. Simulation results for gain, input matching, and noise figure for both bands, verifying switching functionality and specifications.

### C. Active Inductor

Two active inductors were designed for this project, one for each band. The lower frequency inductor achieved 4.59nH with $-0.024\Omega$ series resistance (Q = 27.7) and $2.67\text{nV}/\sqrt{\text{Hz}}$ rms noise at 881MHz. These results are plotted in Fig. 7. Note that in order to compensate for the possibility of instability due to the negative resistance, a small external resistor can be added.



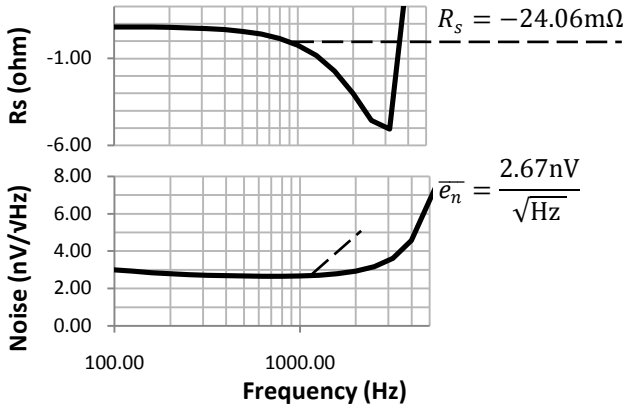



Fig. 7. Simulation results for GSM-850 band active inductor load with values at 881MHz listed.

The higher frequency LNA requires the active inductor load to have a lower rms noise voltage due to the fact that the gain is not as high. In order to achieve the desired noise performance, the M3 cascode transistor was removed, degrading the quality factor of the high frequency active inductor. The inductor was designed as 3.38nH with 33.0Ω series resistance (Q = 1.3) and 2.35nV/$\sqrt{\text{Hz}}$ rms noise at 1.96GHz. The plots for this inductor are shown in Fig. 8. One important difference to note is that the values are flatter to higher frequencies, so that the response will be less distorted at 1.96GHz than if the other active inductor were used.

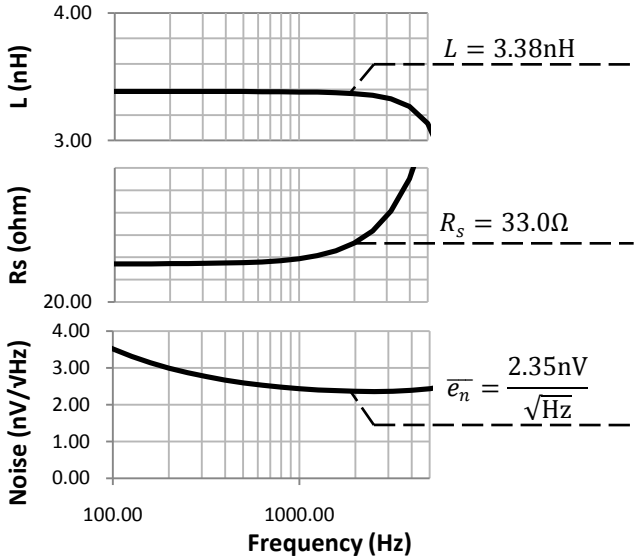



Fig. 8. Simulation results for GSM-1900 band active inductor load with values at 1.96GHz listed.

## IV. Layout

The full layout is shown in Fig. 9. The total area is 0.301mm$^2$.

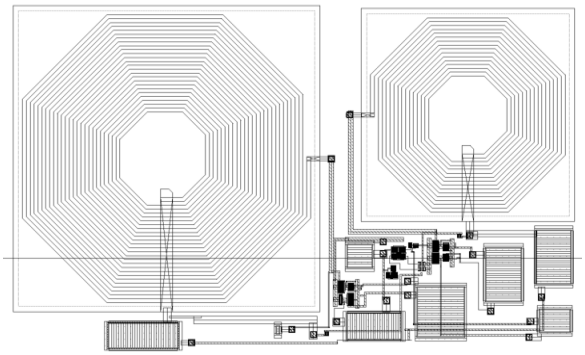


Fig. 9. Chip layout of full system

## V. Summary

In this project, a low-area dual-band LNA for GSM-850 and GSM-1900 was presented. To reduce area, load resonant inductors were replaced by active inductors implemented with gyrator capacitance-to-inductance inverters. Integrated switching capabilities allow the reduction of external noisy input switches.

## References

[1] "3GPP TS 45.005 V8.4.0," Technical Specification Group GSM/EDGE, Radio Access Network; Radio transmission and reception. Feb 2009.

[2] R. Ramzan, S. Andersson, J. Dabrowski, and C. Svensson, "A 1.4V 25mW inductorless wideband LNA in 0.13um CMOS," *ISSCC Dig. Tech. Papers*, 2007, pp. 424-613

[3] D. Shi, N. Behdad, J. Chen, M.P. Flynn, "A 5GHz fully integrated super-regenerative receiver with on-chip slot antenna in 0.13um CMOS," *VLSI Circuits Symposium*, Jun 2008

[4] Thanachayanont, A.; Payne, A., "VHF CMOS integrated active inductor," *Electronics Letters* , vol.32, no.11, pp.999-1000, 23 May 1996

[5] Zhuo, W.; de Gyvez, J.P.; Sanchez-Sinencio, E., "Programmable low noise amplifier with active-inductor load," *Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on* , vol.4, no., pp.365-368 vol.4, 31 May-3 Jun 1998