WCDMA Direct-Conversion Front-End with On-Chip LO in 0.13 µm CMOS

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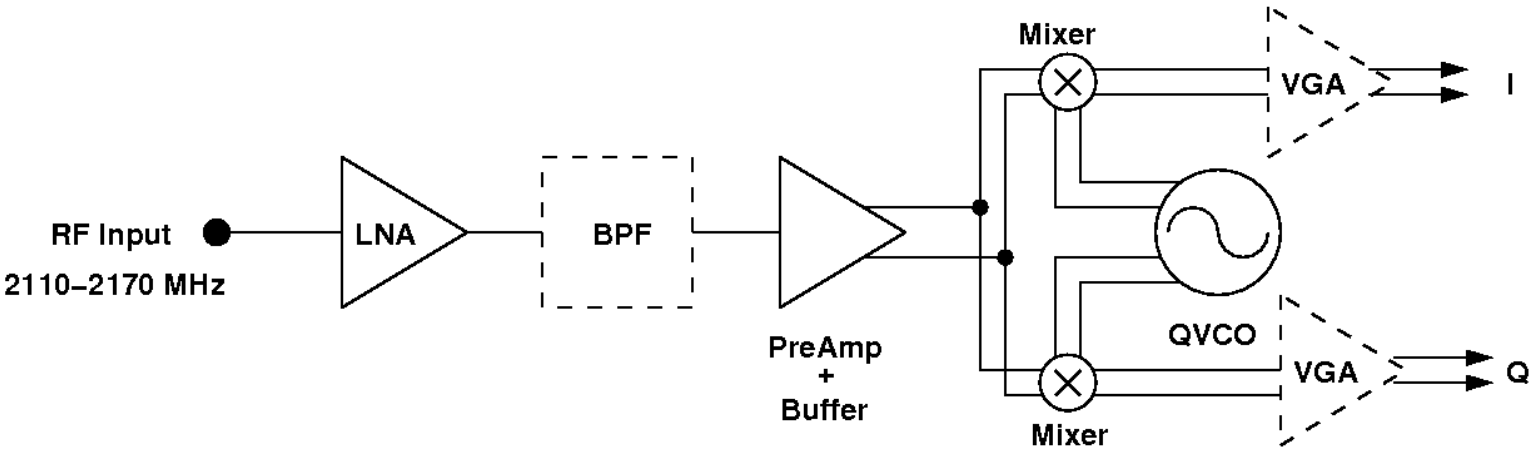
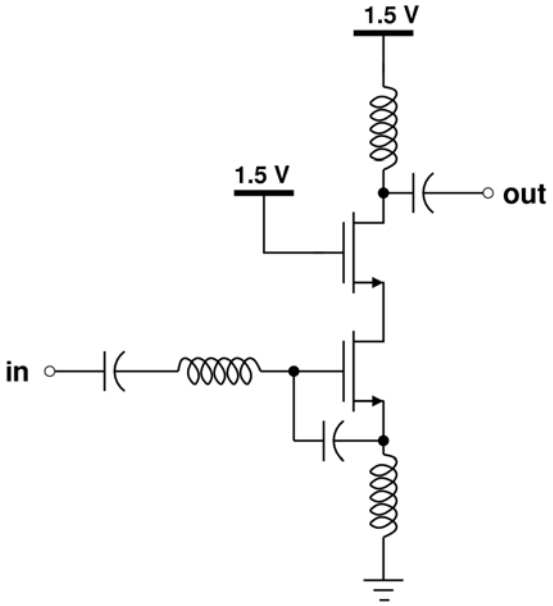
Project Choice

WCDMA Direct Conversion Receiver

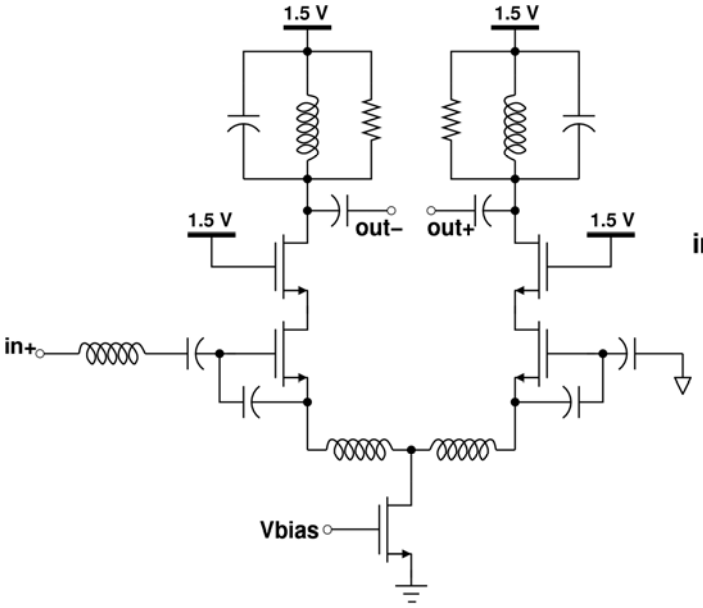


- 3G Telephony standard requiring high linearity and sensitivity requirements
- Few integrated QVCOs in Literature [11]

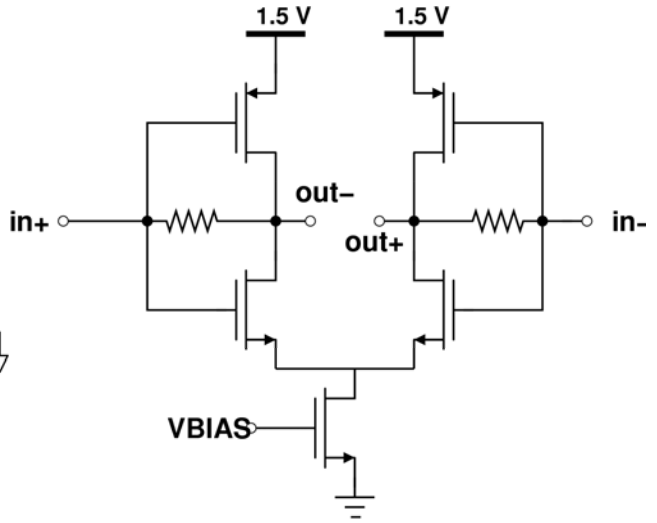
Gain Stages



LNA



Preamplifier



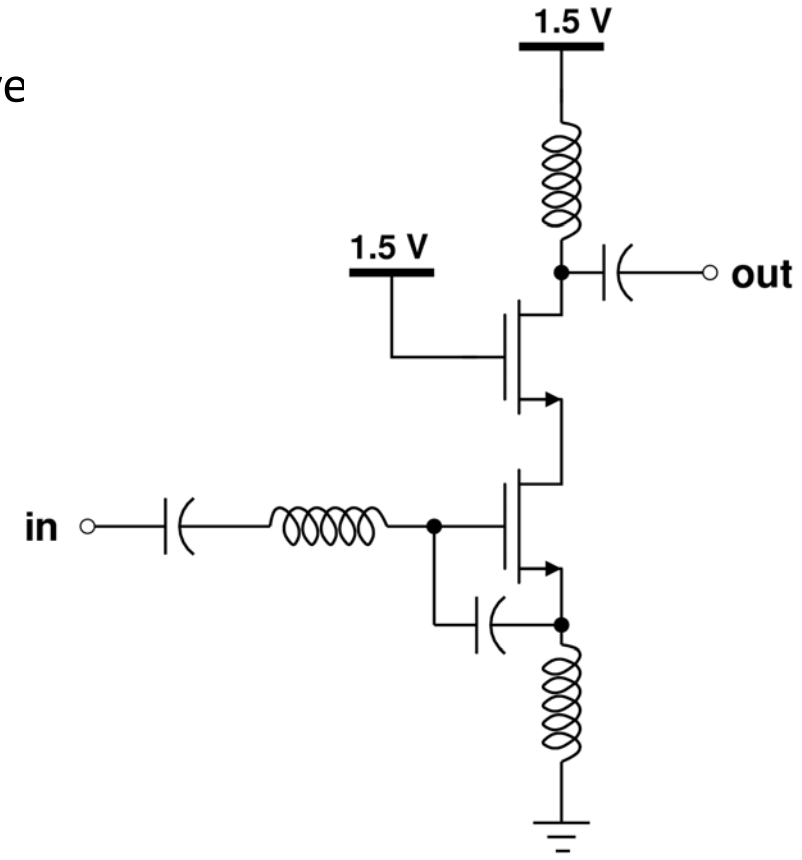
Buffer

Gain Stages consist of LNA, Preamplifier, Buffer

Gain Stages

LNA

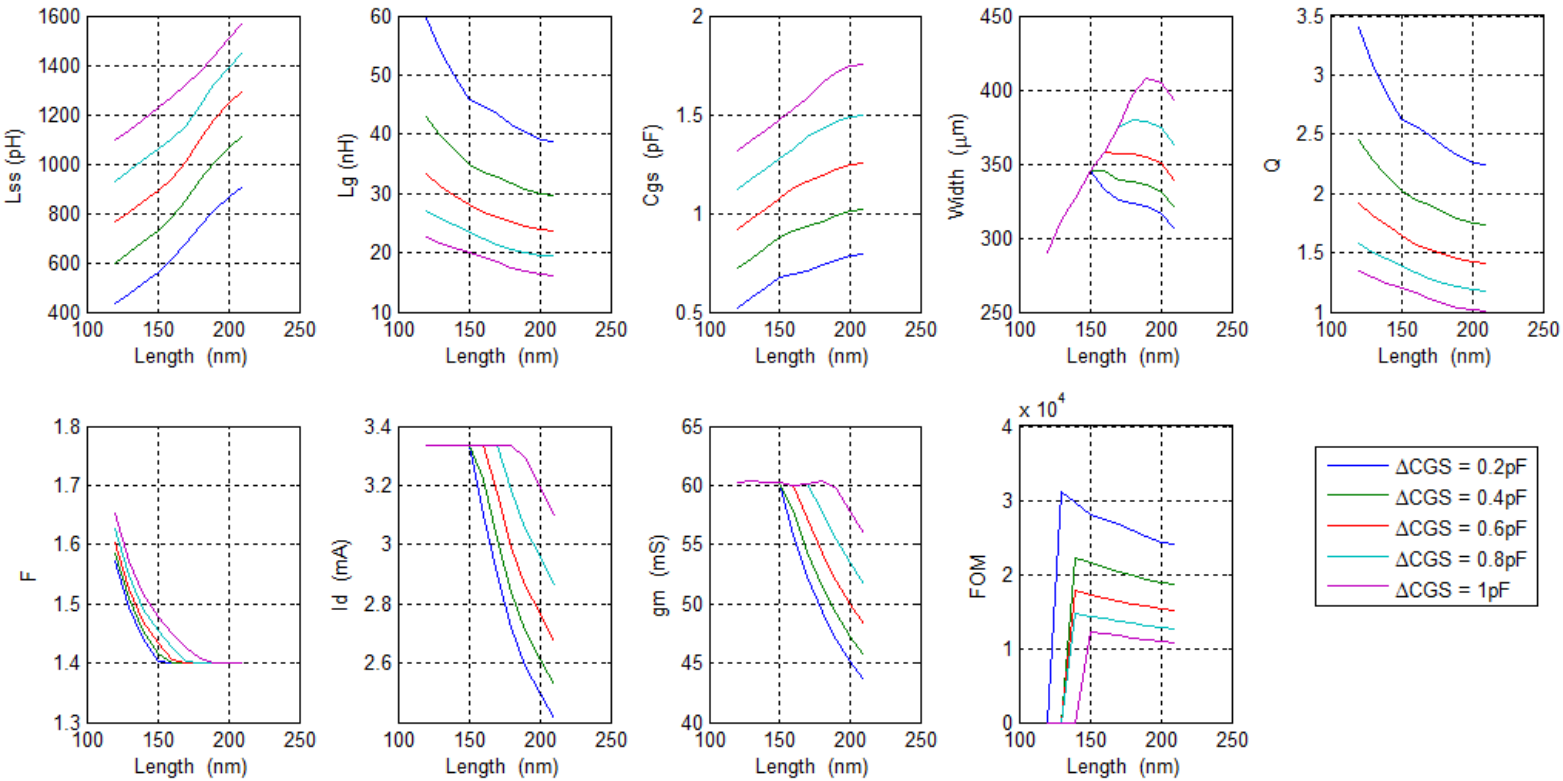
- common source amplifier with inductive degeneration
- Input and Output Impedance matching
- Designed with same methodology as in CAD assignment 2 using MATLAB



$$Zin = j\left(\omega Lss - \frac{1}{\omega Cgs}\right) + gm\frac{Lss}{Cgs}$$

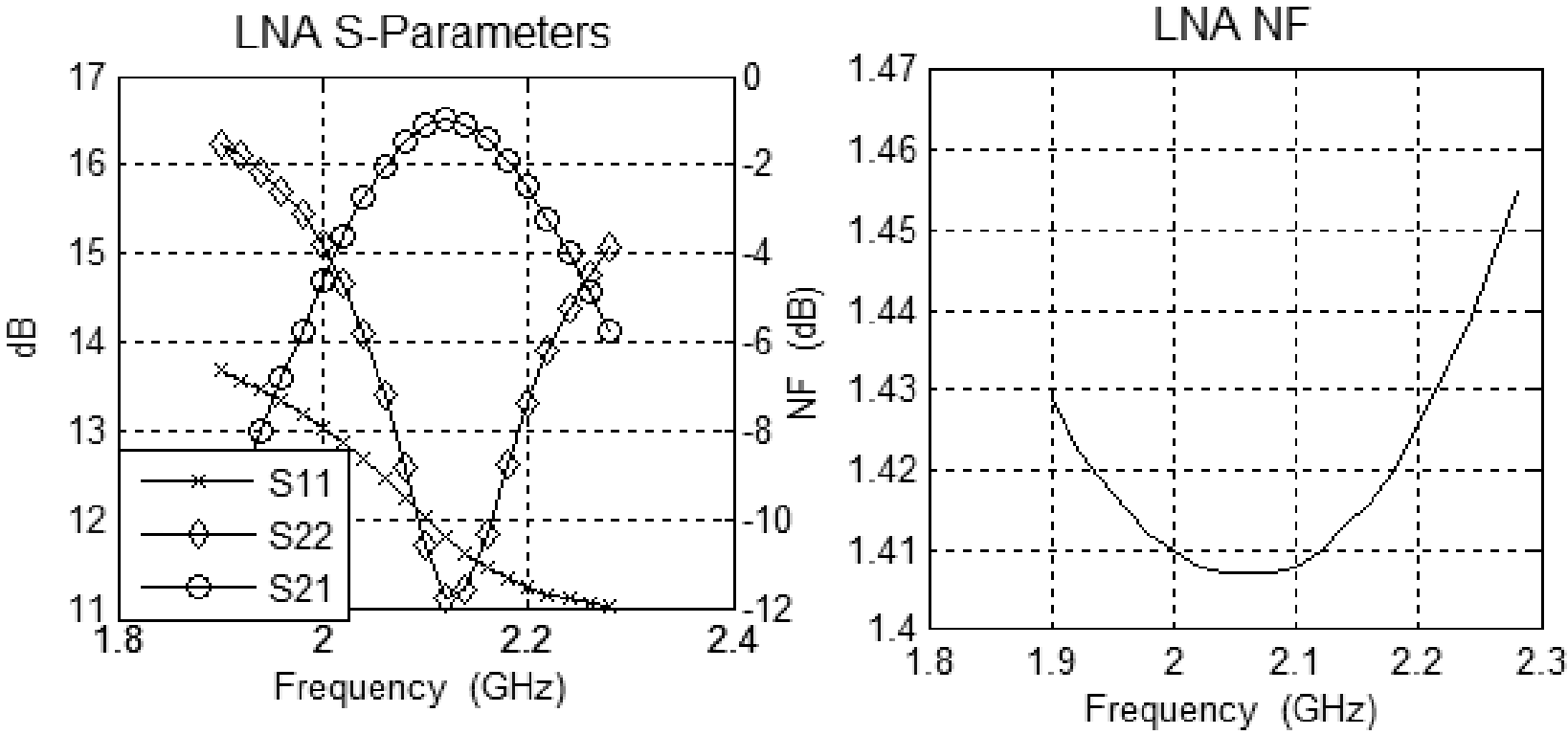
$$F = 1 + k\left(\frac{\omega_O}{\omega_T}\right)\frac{\gamma}{\alpha}\frac{1}{2Q} \qquad Q = \frac{1}{2R_s\omega_0 C_{GS}}$$

Gain Stages



MATLAB plots used to generate design data for LNA

Gain Stages



LNA S-Parameters and Noise Figure

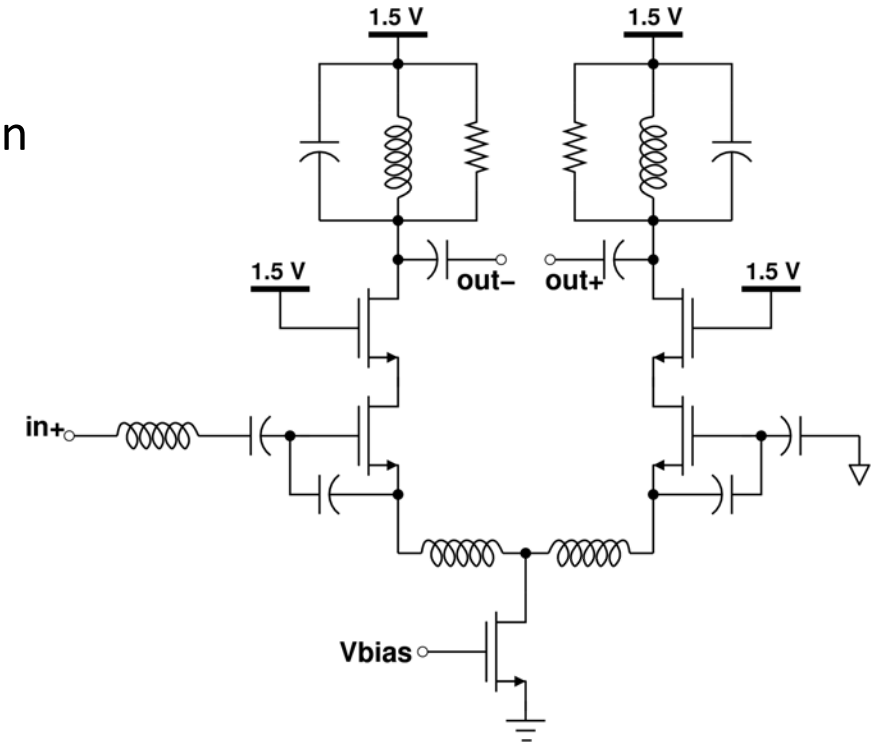
Gain Stages

Preamp

- Single Ended to Differential Conversion
- Input Impedance Matching

$$Zin = j\left(\omega Lg - \frac{1}{\omega Cgs}\right) + gm\frac{Z_{DEG}}{j\omega Cgs} + Z_{DEG}$$

$$Z_{DEG} \approx 2j\omega Lss + \frac{1}{j\omega Cgs} \,||\, \frac{1}{gm}$$



- Output Balancing

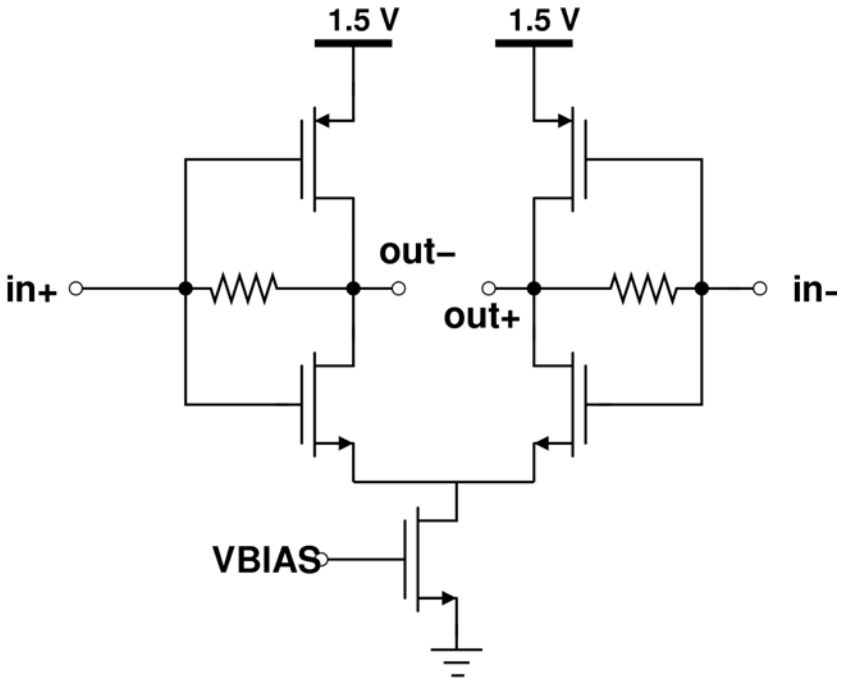
$$out^- = -out^+ - gmR\left[1 + \omega^2 2L_{SS}C_{gs} - 2j\omega gmL_{SS}\right]Vin$$

$$out^+ = \frac{gmR}{j\omega 2R_sC_{gs}}Vin$$

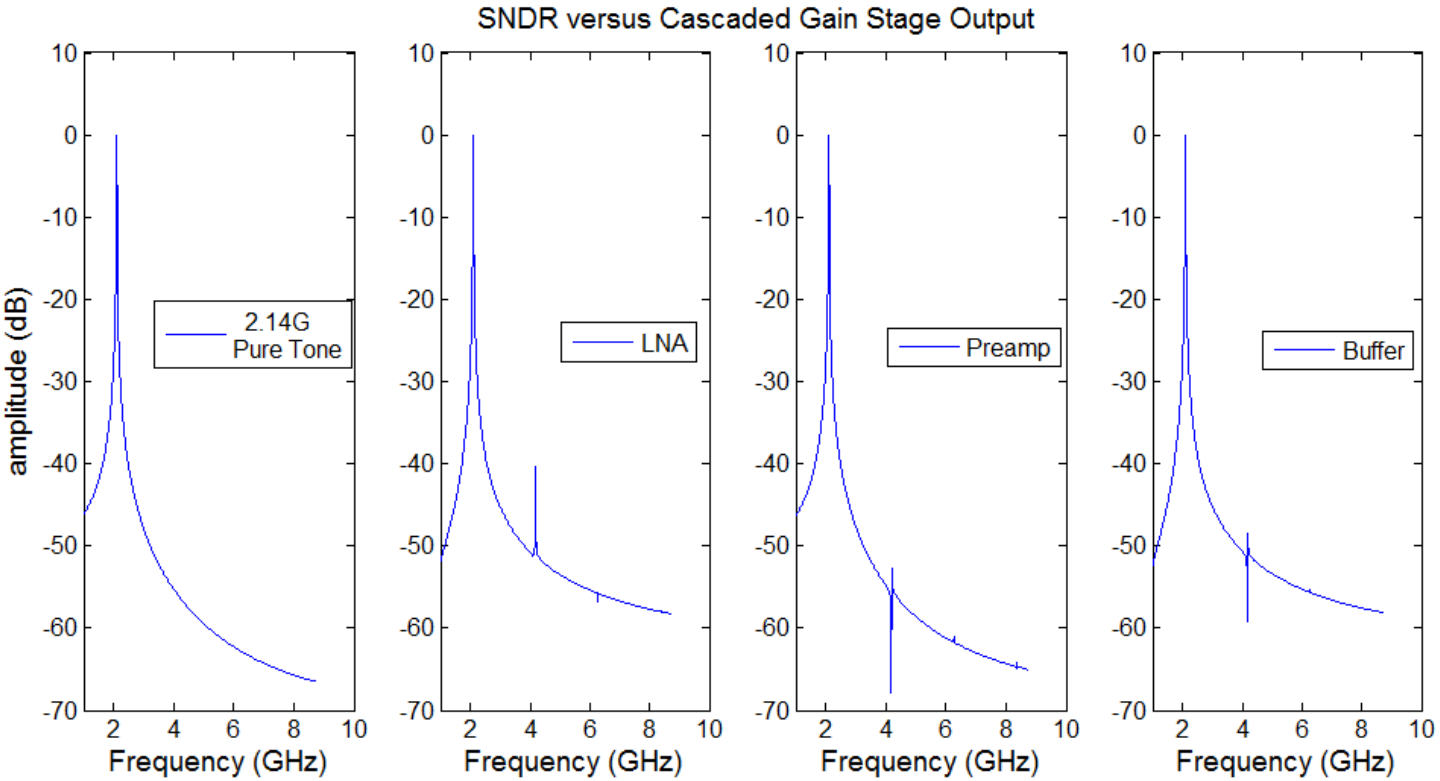
Gain Stages

Buffer

- Self Biasing
- Helps Isolate Preamp from LO
- Cool Little Circuit



Gain Stages



SNDR at Gain Stage Outputs

Gain Stages

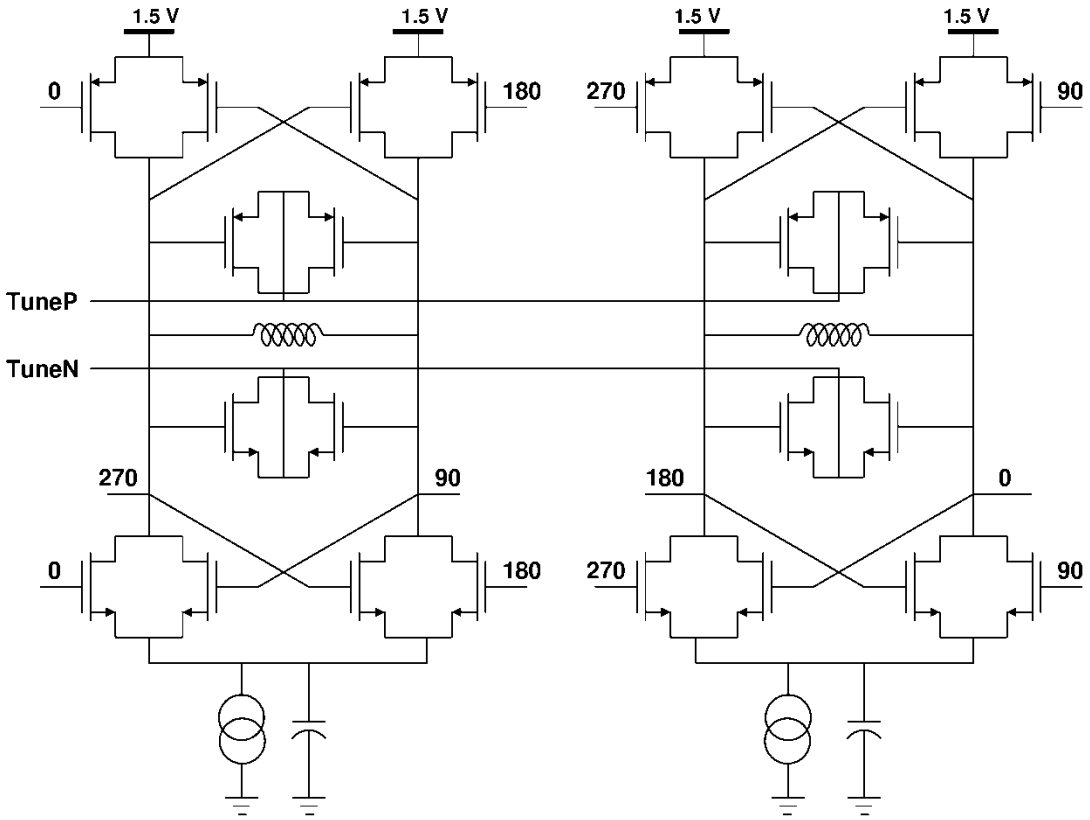
LOW NOISE AMPLIFIER PERFORMANCE TABLE

	Specification	Targeted	**Simulated**
LNA	NF	< 1.5 dB	**1.42 dB***
	Gain	> 15 dB	**16.5 dB**
	P1dB	> -15 dBm	**-9.33 dBm**
	IIP3	> -15 dBm	**-5.62 dBm**
	S11	< -10 dB	**-10 dB**
	S22	< -10 dB	**-12 dB**
	Current	< 5mA	**3.768mA**
PREAMP **	NF	< 2 dB	**3.663 dB ***
	Gain	> 8 dB***	**11 dB*****
	P1dB	> -5 dBm	**-8.3 dBm**
	IIP3	> -15 dBm	**-0.9 dBm**
	S11	< -10 dB	**-8.6 dB**
	Current	< 8mA	**12.5mA**

* simulated values do not include correlated gate noise.
** simulated values include both Preamplifier and Buffer
*** measured differentially

Quadrature VCO Design (1)

- Topology: tail current-source biased LC QVCO
  - Rail-to-rail swing
  - Low VDD operation



Quadrature VCO Design (2)

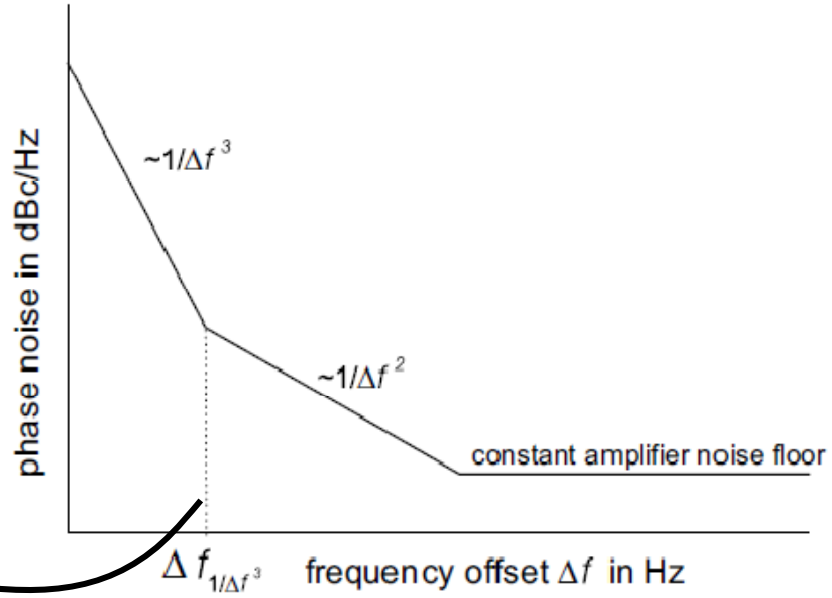
- Basic VCO Phase Noise LTI Model

$$\mathcal{L} = 10\log\left[\frac{2FkT}{P_{sig}}\left(\frac{\omega_c}{2Q_{tank}\Delta\omega}\right)^2\right]$$

Quadrature VCO Design (3)

- Hajimiri's VCO Phase Noise Model for $1/f^3$ Corner:

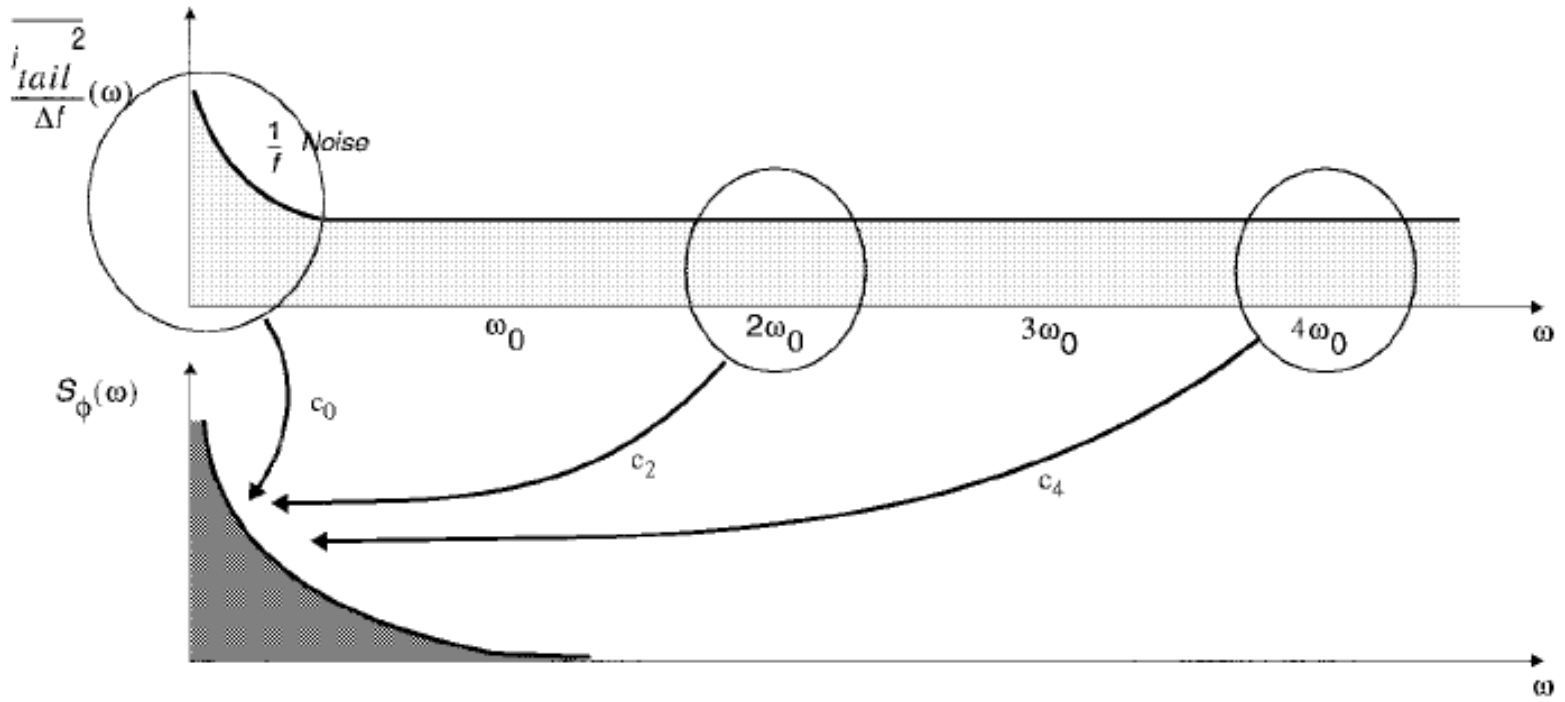
$$\omega_{1/f^3} = \omega_{1/f} \cdot \left(\frac{c_0}{c_1}\right)^2$$



- Equalize Pull-Up and Pull-Down Strength to Maximize Symmetry

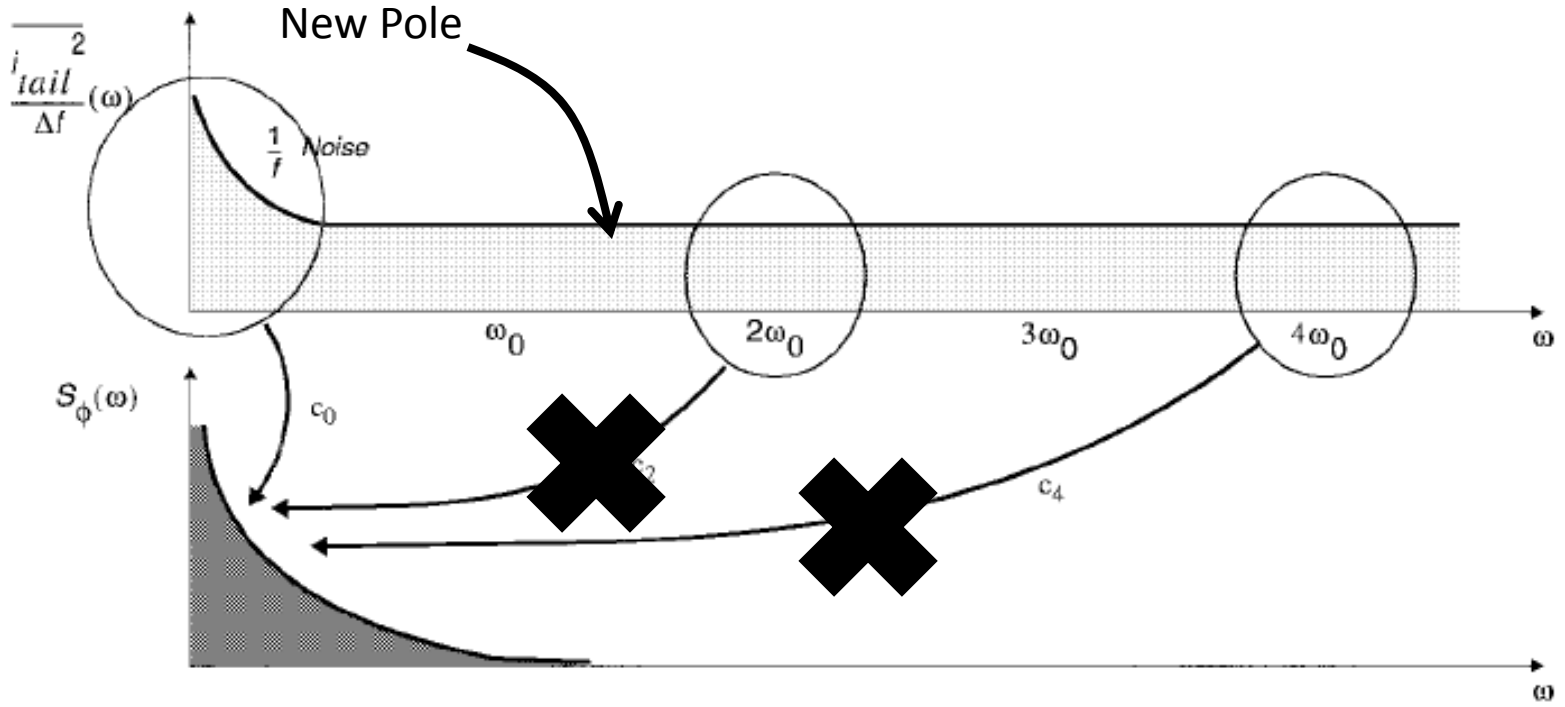
Quadrature VCO Design (4)

- Add a pole to the tail to avoid noise to phase noise conversion at even harmonics



Quadrature VCO Design (5)

- Add a pole to the tail to avoid noise to phase noise conversion at even harmonics

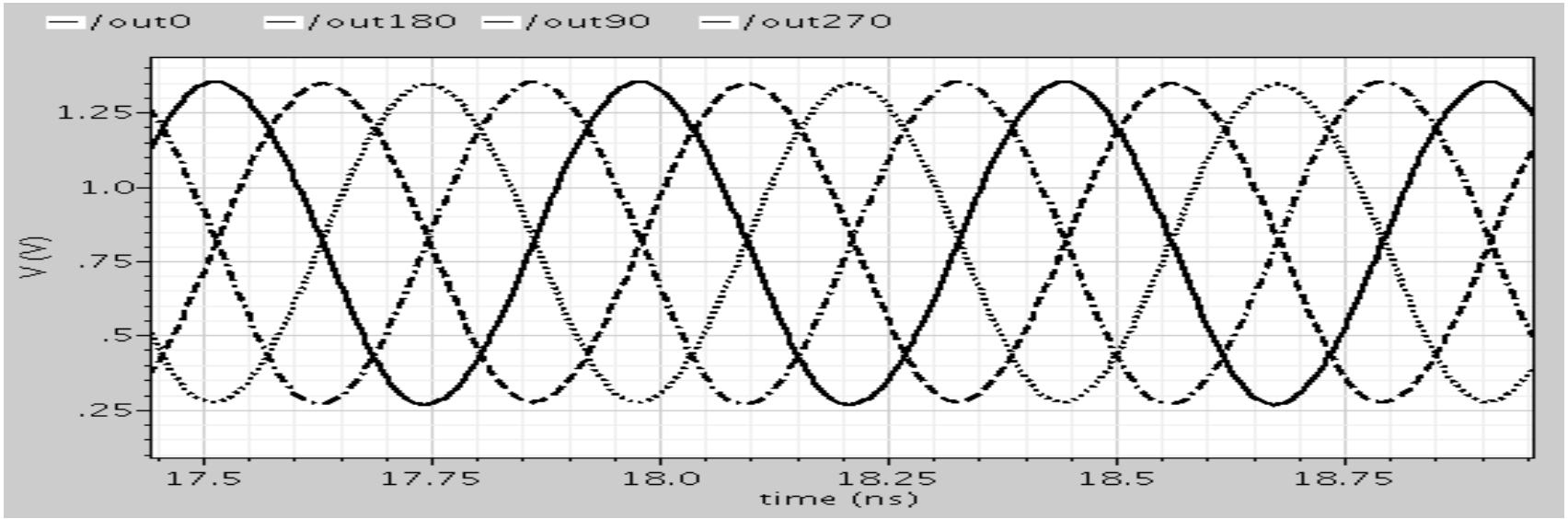


Quadrature VCO Design (6)

OSCILLATOR PERFORMANCE TABLE

Specification	Targeted	**Simulated**	[7]	[8]
Frequency	2.11-2.17GHz	**2.10-2.28GHz**	1.1GHz	1.93GHz
Phase Noise*	< -113	**-124**	-120	-122
Power	< 30mW	**15mW**	5.4mW	27mW
FOM	-170	**-180.8**	-173.5	-171

* computed at 1MHz (dBc/Hz)

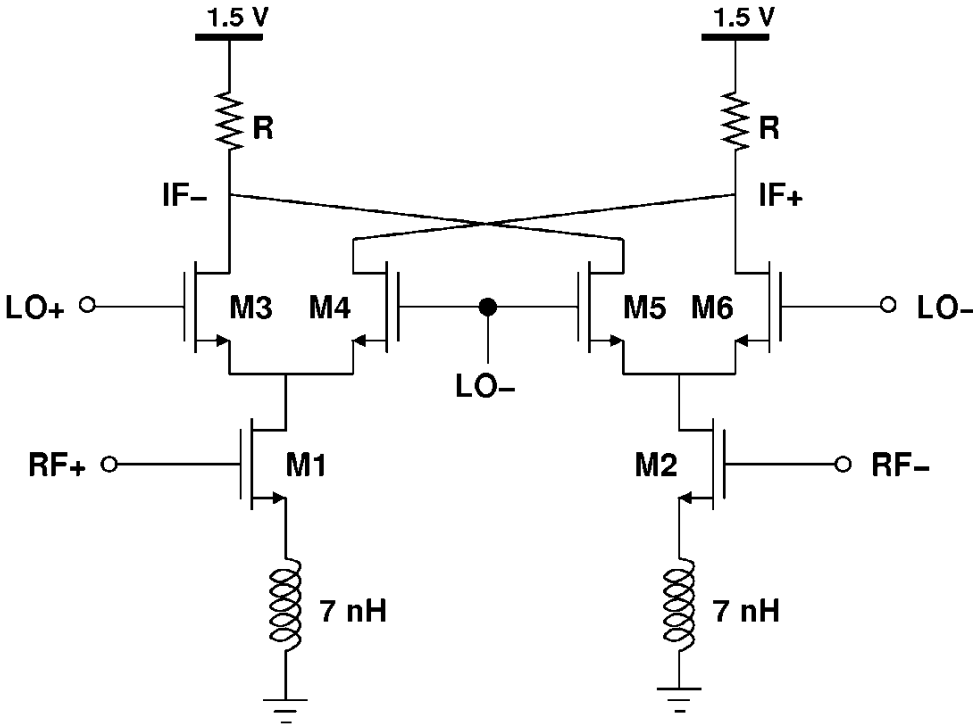


Mixer Design (1)

- Perform Frequency Conversion
- Design Considerations
  - Moderate Gain (not too high to saturate later stages)
  - High linearity for WCDMA applications
  - Low noise figure (NF)
  - Low even order distortions
  - Minimum port-to-port feed-through
- Mixer optimized for high linearity and low NF

Mixer Design (2)

- Linearity better than traditional Gilbert Cell [3]
- Suitable for low VDD process
- Inductor degeneration to enhance linearity.
  - Penalty: Area and Gain
- Switches made big for low R_{ON} and low flicker noise



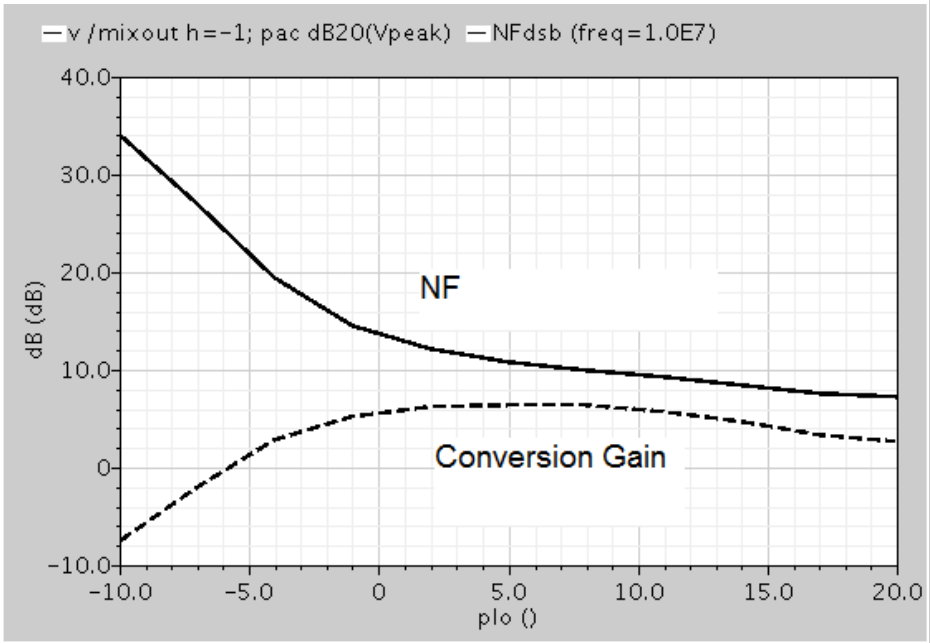
Conversion Gain:

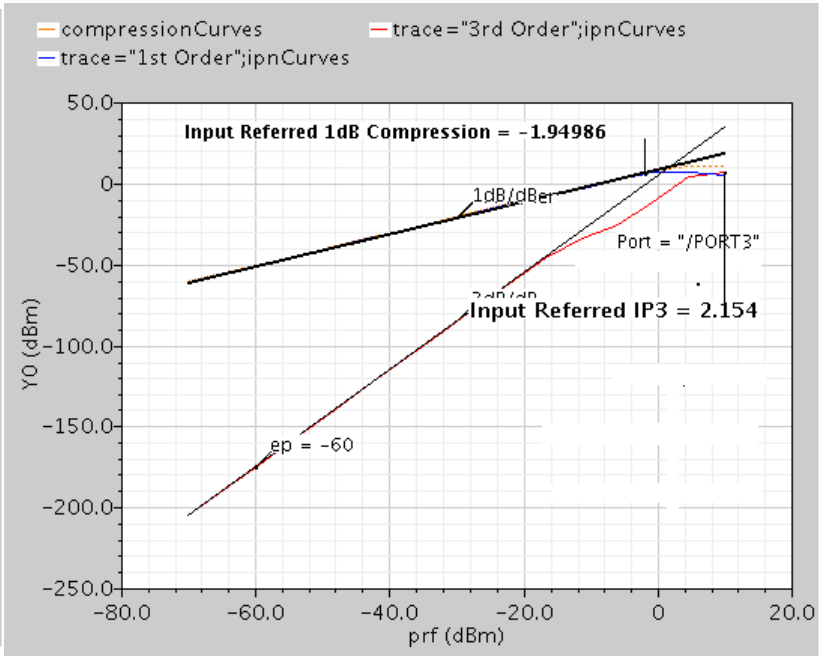
$$CG = \frac{2G_{m,eff}R}{\pi}$$

Output Noise Contribution of M1/2:

$$v_n{}^2 = \frac{4kT\gamma}{gm_{1,2}}\left(\frac{2}{\pi}gm_{1,2}R\right)^2\left(1+\frac{1}{3^2}+\frac{1}{5^2}+\cdots\right)$$

Mixer Design (3)





MIXER PERFORMANCE TABLE

Specification	Targeted	**Simulated**
Conversion Gain	> 2 dB	**8 dB***
NF(dsb)**	< 15 dB	**10 dB**
P1dB	> -5 dBm	**-1.95 dBm**
IIP3	> 0 dBm	**2.154 dBm**
Current	< 10 mA	**10 mA**

* simulated with 5dBm oscillator amplitude

** Dual Side Band, NF(ssb) = NF(dsb) + 3dB

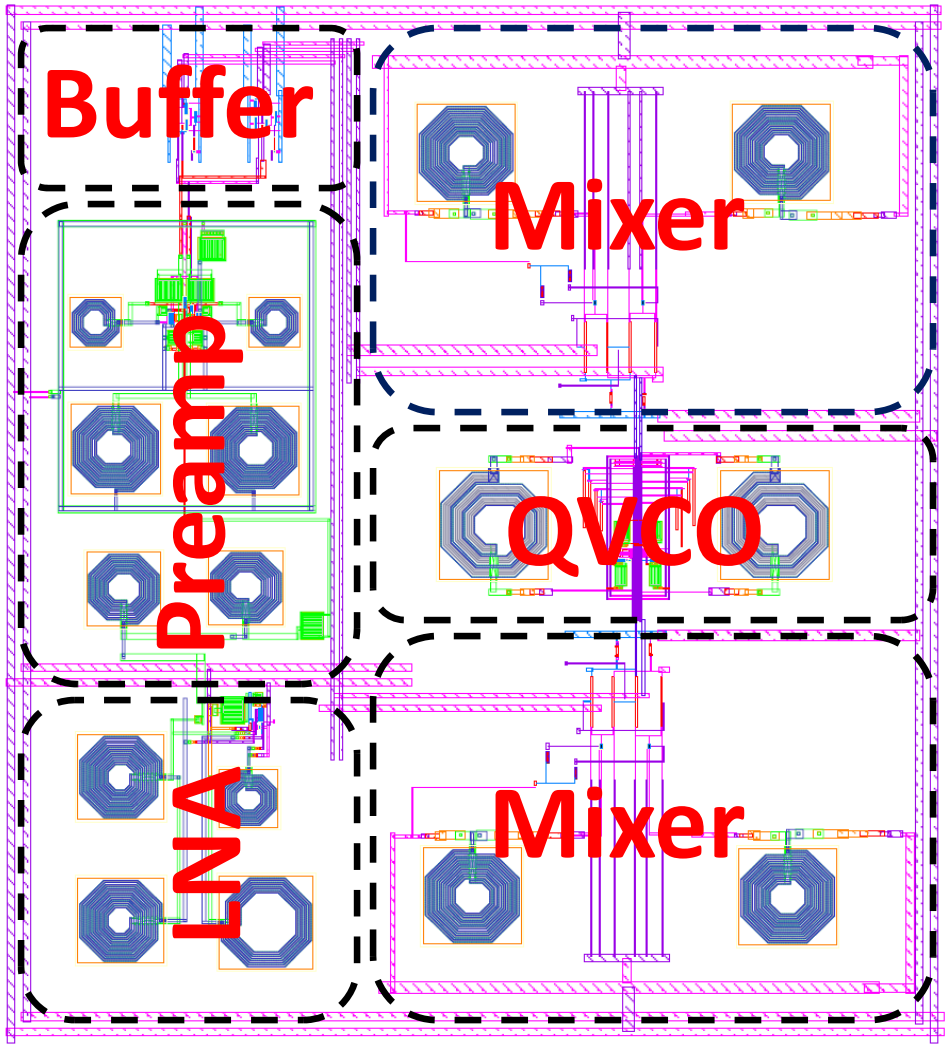
Performance Summary

SYSTEM PERFORMANCE TABLE

Specification	Targeted	**Simulated**	[9]	[10]	[11]
Process (um)	0.13	**0.13**	0.25	0.13	0.18
NF (dB)	< 6	**1.96***	8.92	--	--
NFdsb (dB)	--	**1.56**	--	6.5	5.6
Gain (dB)	> 25	**44** **	16.92	34.8	47
P1dB (dBm)	> -25	**-4.39**	-21.1	-24	--
IIP3 (dBm)	> -25	**-0.98**	-15.04	-8.6	-10
Power (mW)		**58.2**	72.15	73	--
(w/VCO)	< 60	**73.2**	--	--	37.8
Phase Noise***	< -113	**-124**	--	--	-155

* computed using Friis equations -- provided for comparison purposes
** simulated with QVCO from transient analysis
*** computed at 1MHz (dBc/Hz)

Layout



2.4mm x 2.6mm

REFERENCES

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[2] R. Fiorello, "Common Gate LNA Design Space Exploration in All Inversion Regions," Proceedings of the Argentine School of Micro-Nano-electronics, Technology and Applications 2008

[3] C. Toumaz et at, "Trade-offs in analog circuit design: the designers companion", Kluwer Academic Publishers, 2002.

[4] P. Andreani et al. "Analysis and Design of a 1.8-GHz CMOS LC Quadrature VCO", JSSC 2002

[5] M. Tiebout "Low Power VCO Design in CMOS", NY, Springer 2006

[6] A. Hajimiri et al. "Design Issues in CMOS Differential LC Oscillators", JSSC 1999

[7] H. Kim, "A Very Low-Power Quadrature VCO with Back-Gate Coupling", JSSC 2004

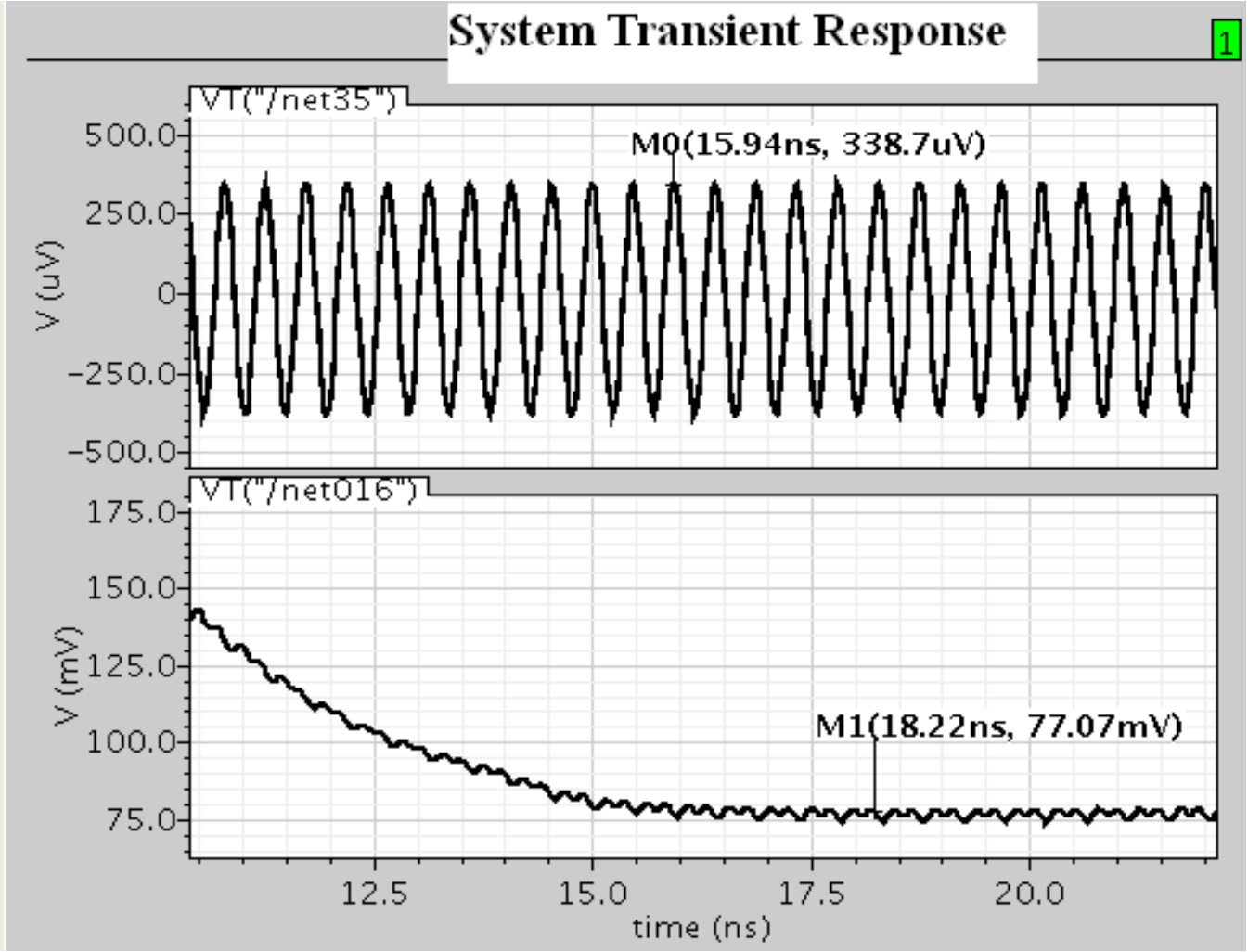
[8] A. M. ElSayed and M. I. Elmasry, "Low-phase-noise LC quadrature VCO using coupled tank resonators in a ring structure," *IEEE J. Solid-State Circuits*, vol. 36, pp. 701-705, Apr. 2001.

[9] M Adeel and C. Lee, "WCDMA Direct Conversion Receiver Front End," University of Michigan, EECS 522, Final Project Report, Winter 2008, http://www.eecs.umich.edu/courses/eecs522/w08/Reports/... group3_report.pdf

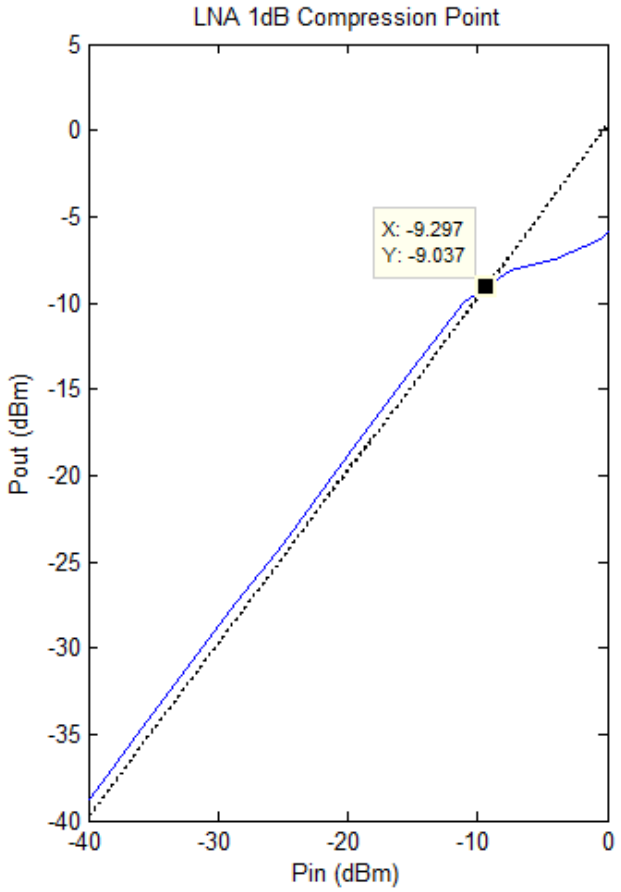
[10] J. Rogin, I. Kouchev, G. Brenna, D. Tschopp, and Q. Huang, "A 1.5-V 45-mW direct-conversion WCDMA receiver IC in 0.13-_m CMOS,"*IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2239–2248, Dec. 2003.

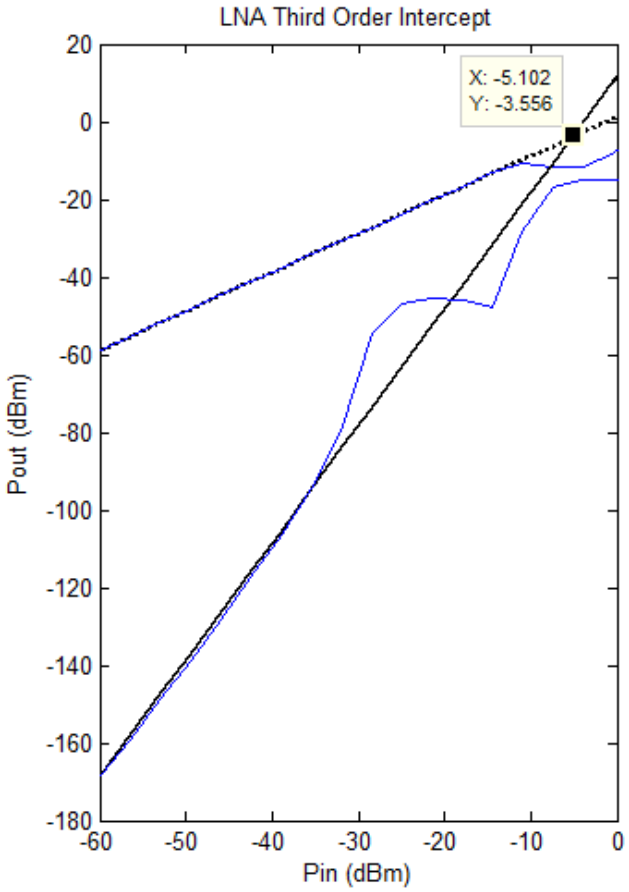
[11] F. Gatta, D. Manstretta, P. Rossi, and F. Svelto, "A fully integrated for 0.18-_m CMOS direct conversion receiver front-end with on-chip LO UMTS," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 15–23, Jan.

Appendix (Transient Response)



Appendix


LNA 1dB Compression Point
X: -9.297
Y: -9.037
Pout (dBm)
Pin (dBm)
5
0
-5
-10
-15
-20
-25
-30
-35
-40
-40
-30
-20
-10
0


LNA Third Order Intercept
X: -5.102
Y: -3.556
Pout (dBm)
Pin (dBm)
20
0
-20
-40
-60
-80
-100
-120
-140
-160
-180
-60
-50
-40
-30
-20
-10
0